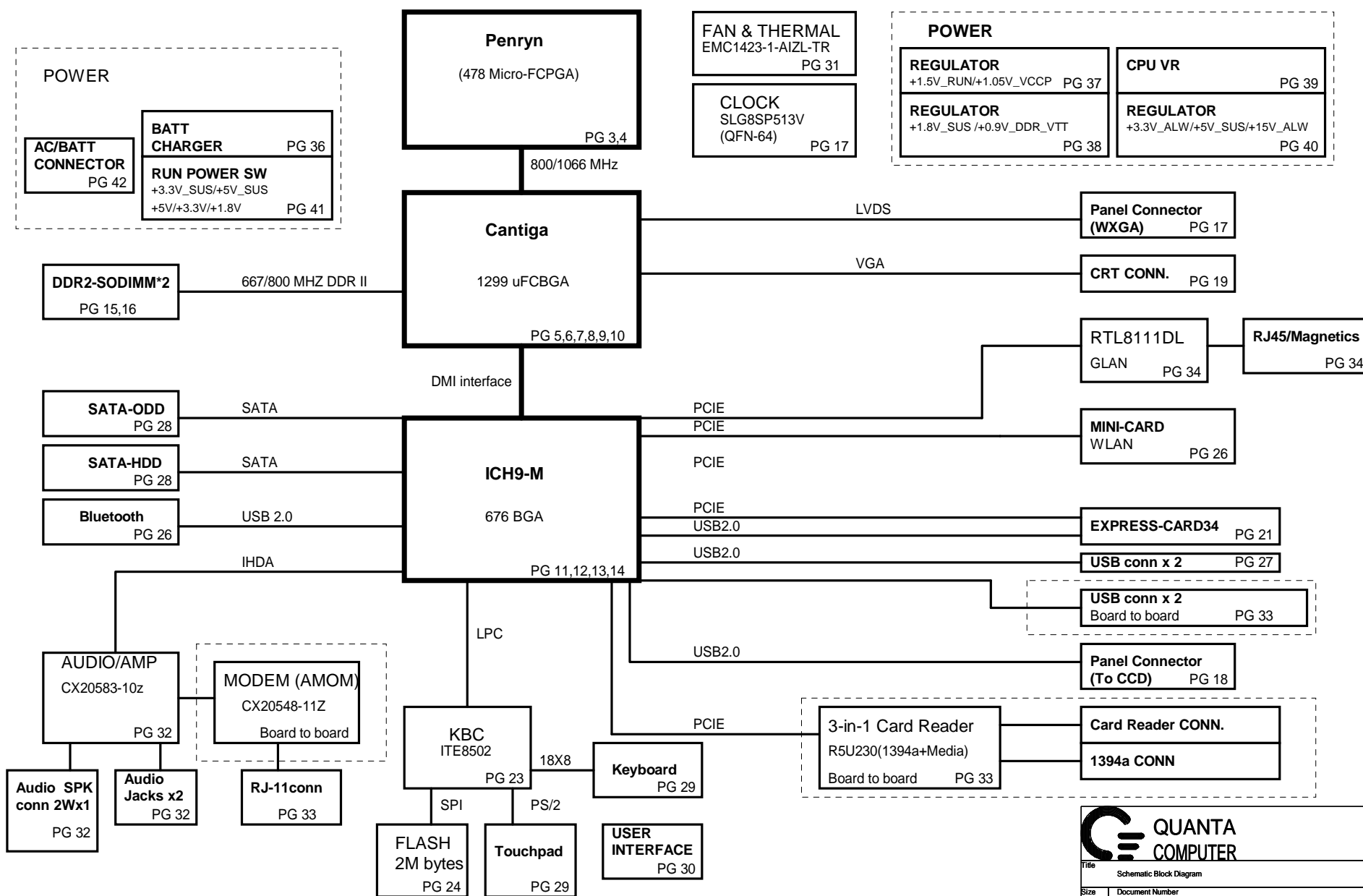


# VM9M Block Diagram Intel UMA




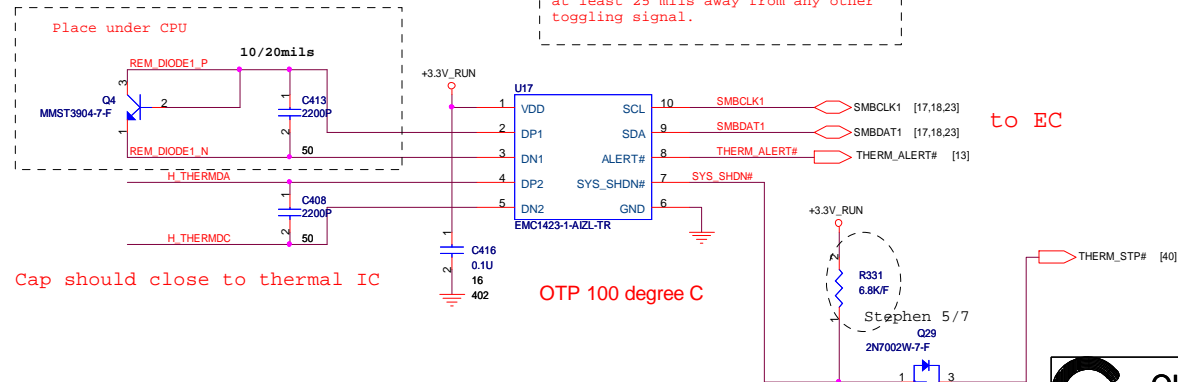
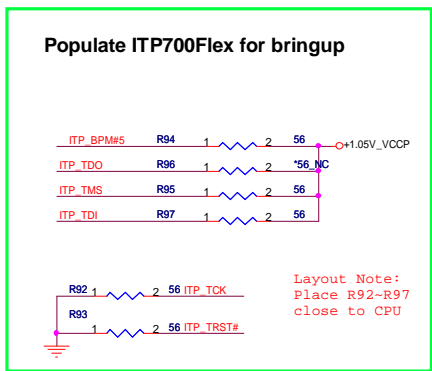
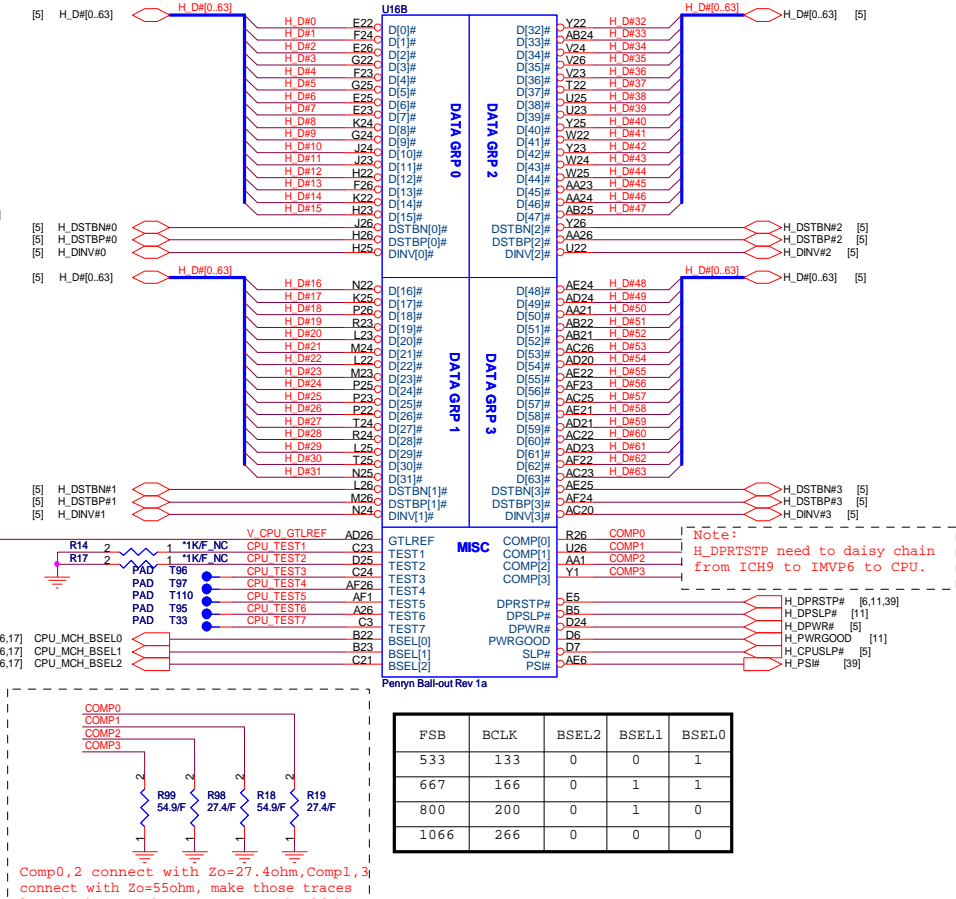
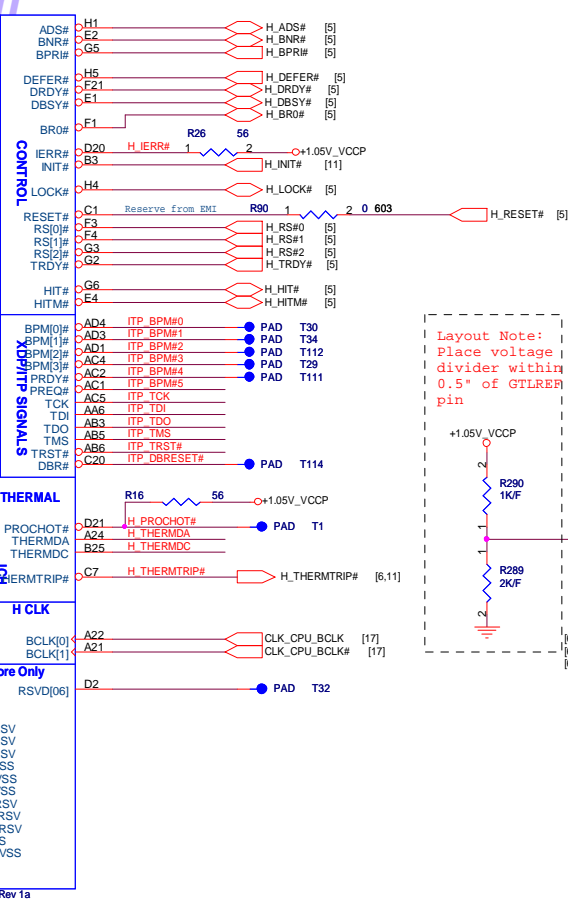
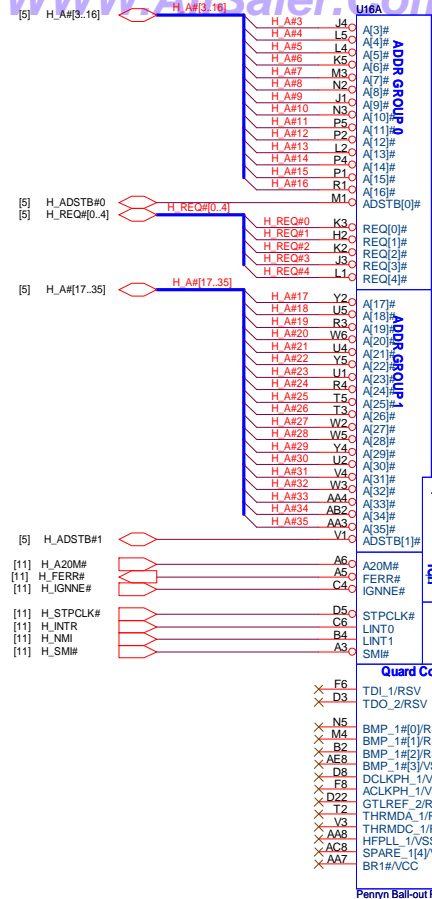
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## Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,18,24,36,37,3,8,39,40,44	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,23,24	RTC		S0~S5
+3.3V_ALW	+3.3V	3,23,24,30,35,36,38,40,41,42,45	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	37,38,40,41,42	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	11,18,40,41	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	34	LAN POWER		
+5V_SUS	+5V	14,27,30,39,40,41,44	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,18,25,30,37,39,41,45	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,37,38,41	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,38,41	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,18,19,21,25,28,29,30,31,32,41,44	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,6,8,9,11,12,13,14,15,17,30,31,32,34,18,19,20,21,23,25,26,28,41,44,45	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,26,37,41,44	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,6,8,9,11,14,37,44	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,39	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	18	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	28	Module Power		
+5V_HDD	+5V	28	HDD Power		
+PBATT	+10V~+17V	42	MAIN BATTERY	CHG_PBATT	

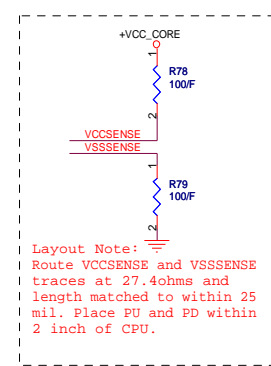
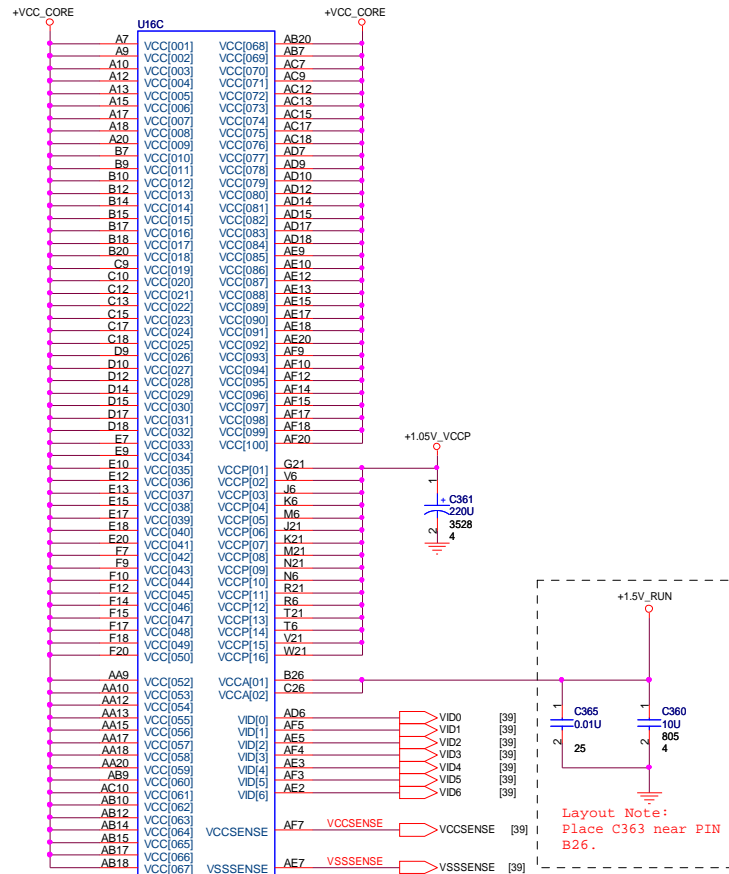
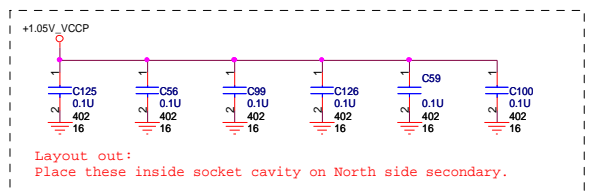
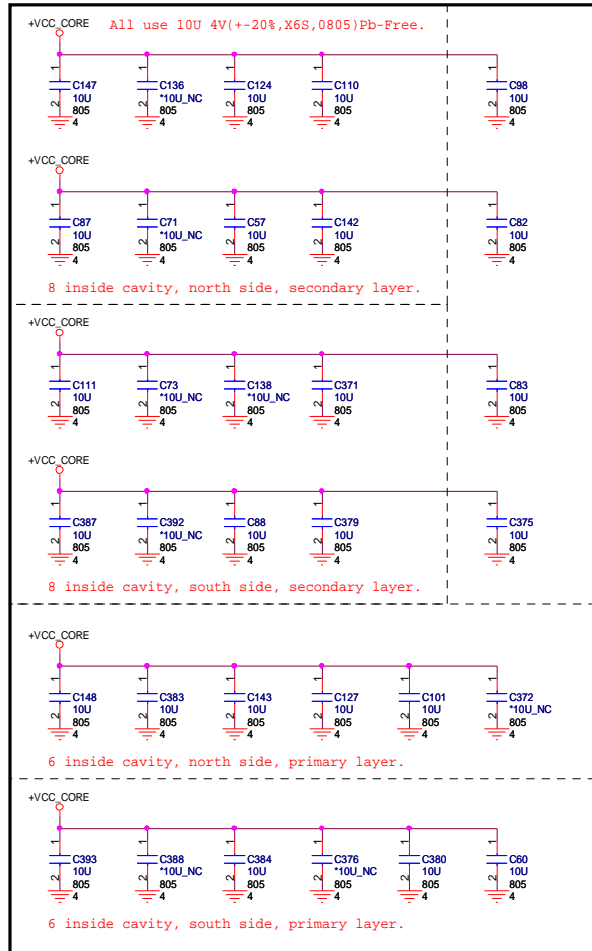
GND PLANE	PAGE	DESCRIPTION
 GND	ALL	

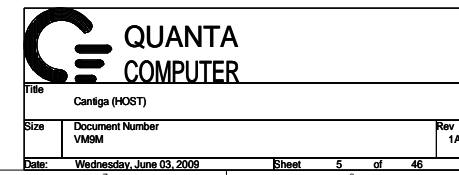


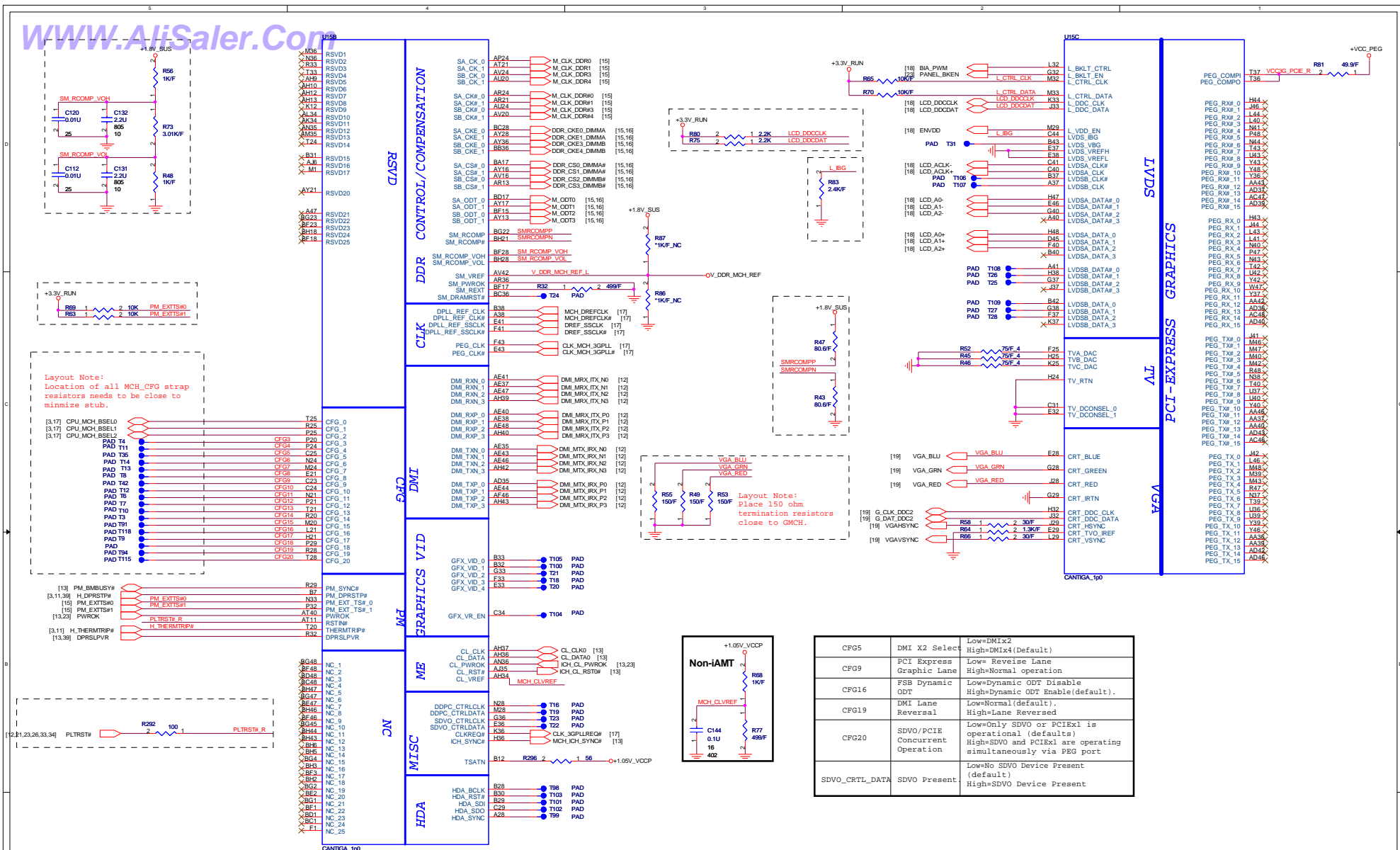
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0

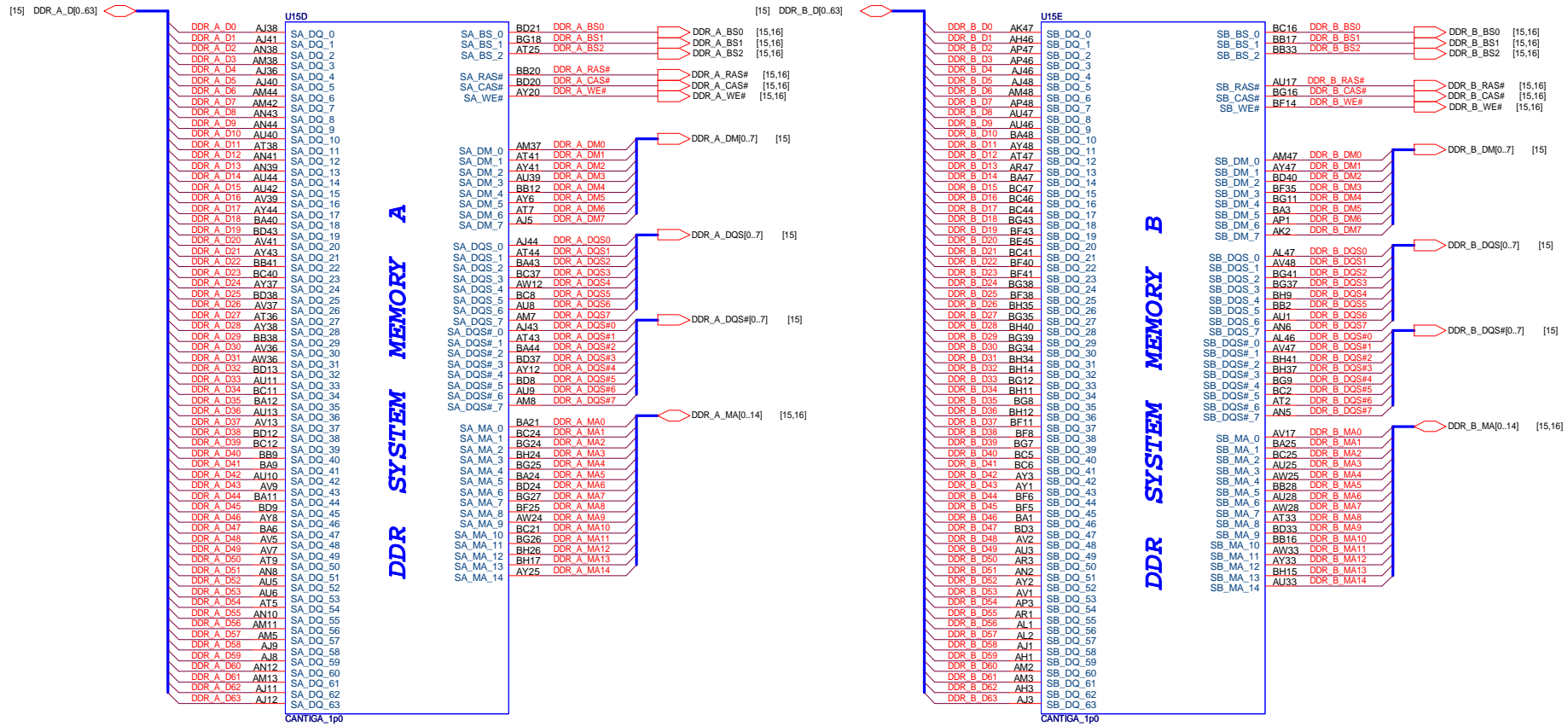


Title			
Penryn Processor (HOST BUS)			
Size	Document Number		Rev
	VMSM		1A
Date:	Saturday, June 06, 2009	Sheet	3 of 46

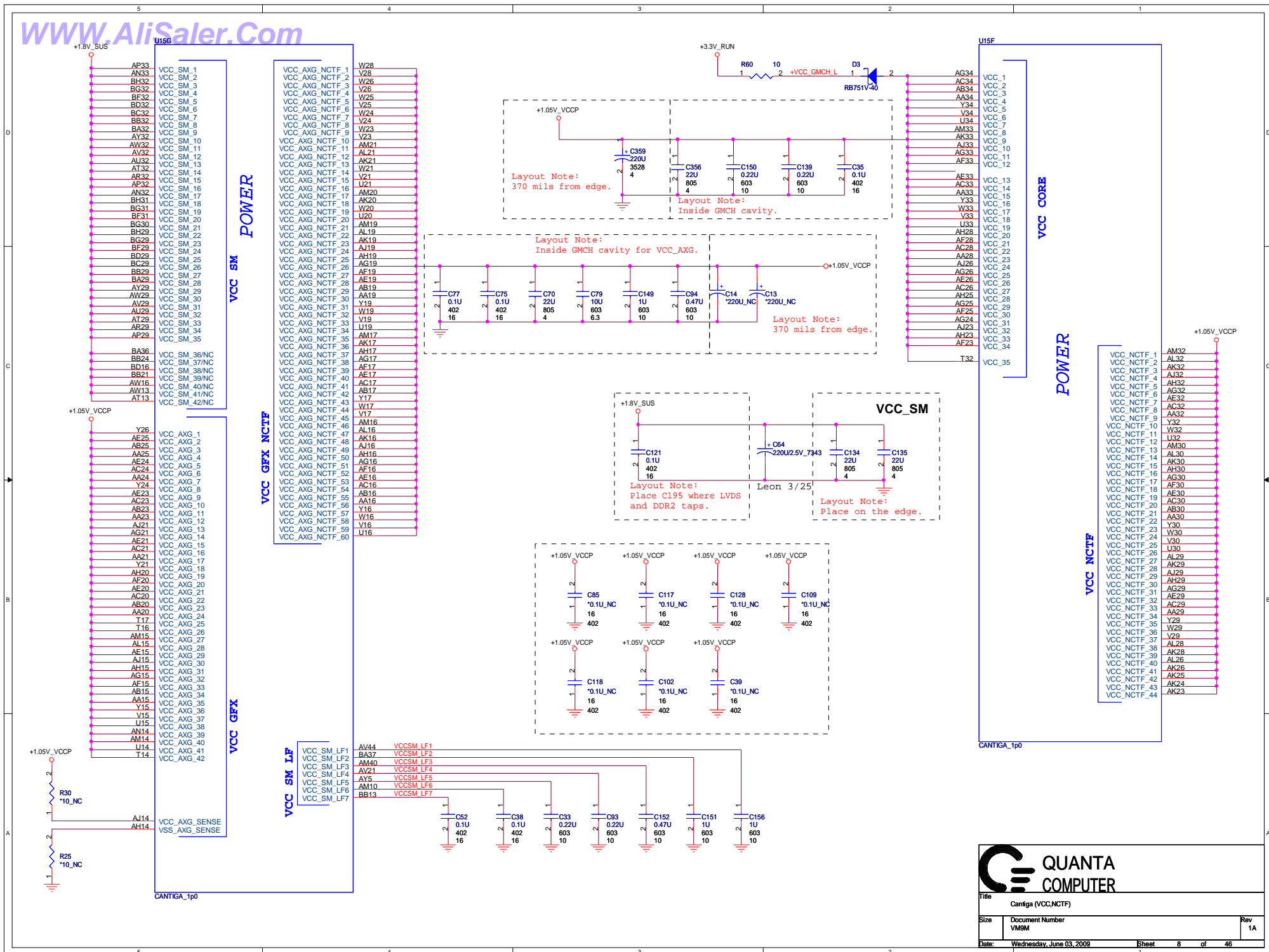




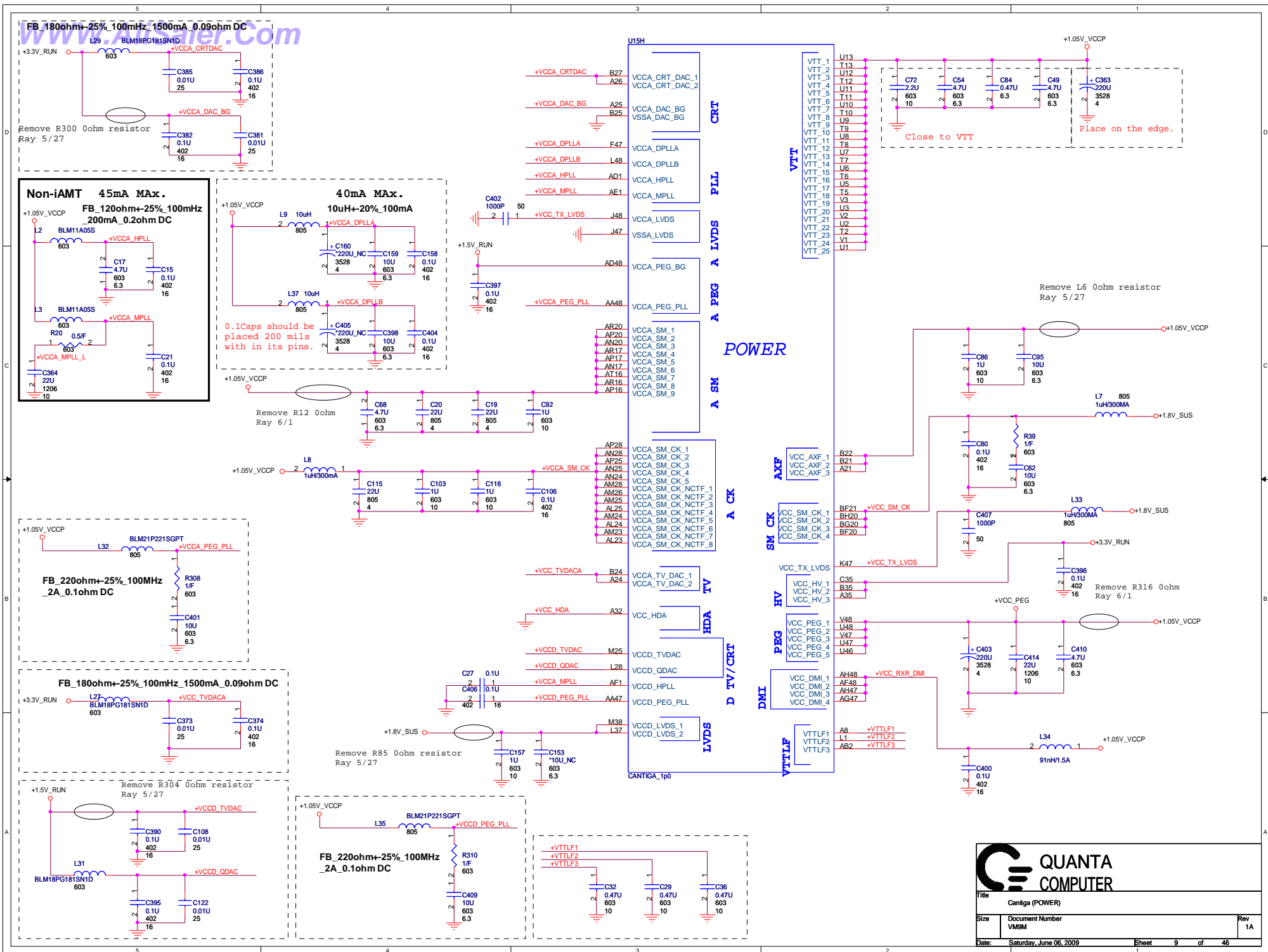


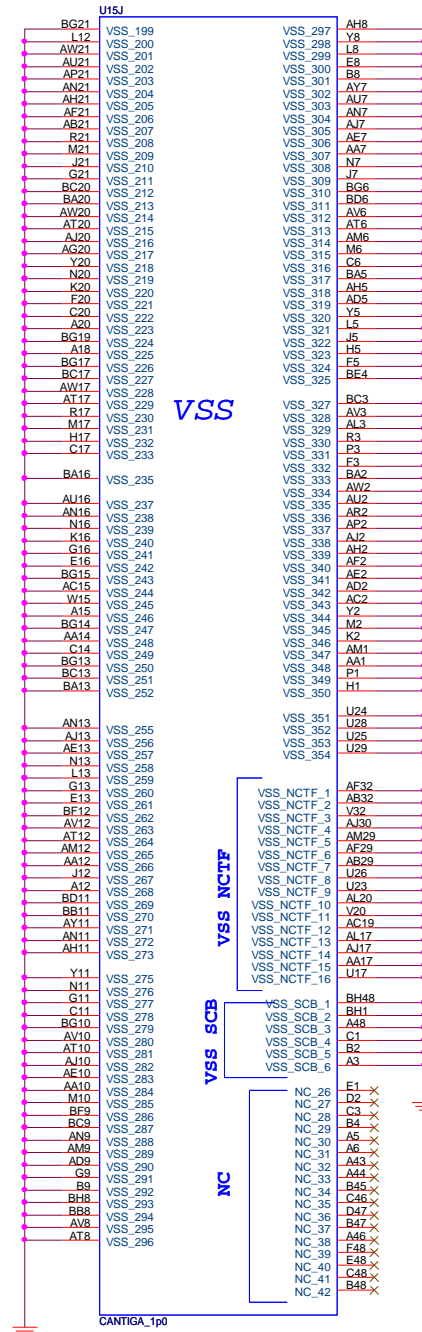
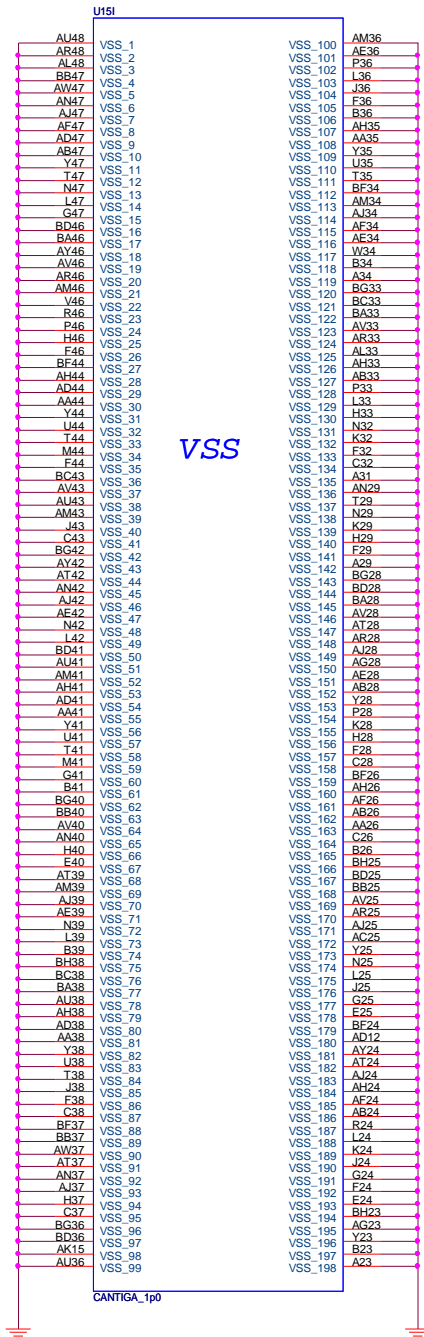





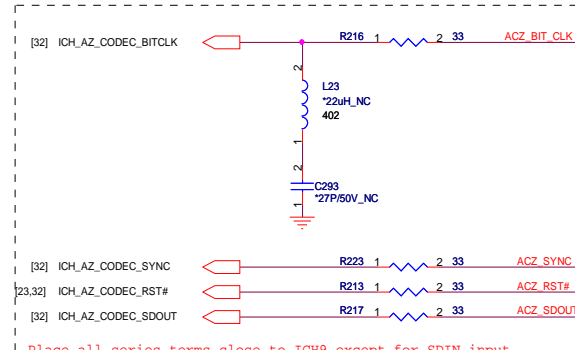
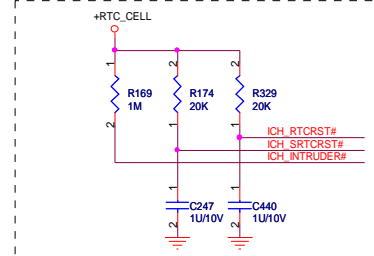
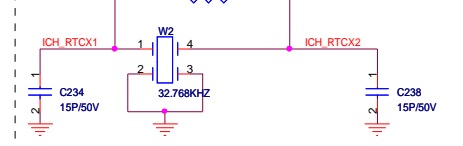




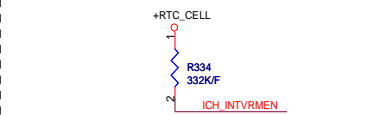
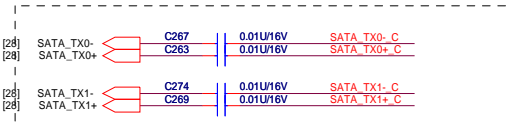




		
Title Cantiga (VSS)		
Size	Document Number VMSM	Rev 1A
Date: Wednesday, June 03, 2009	Sheet 10 of 46	

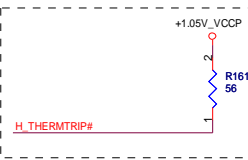
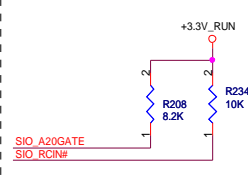
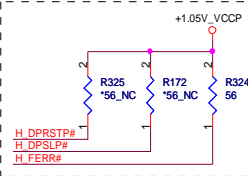
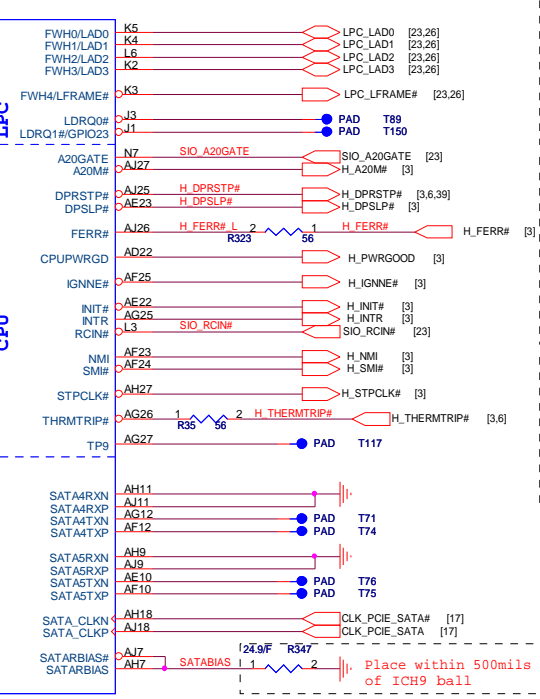
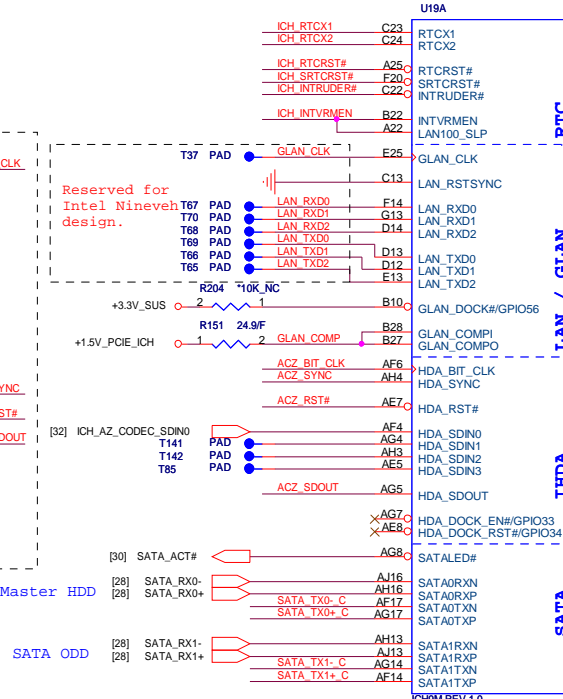


Place all series terms close to ICH9 except for SDIN input lines, which should be close to source.

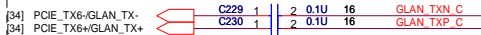


ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

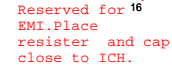
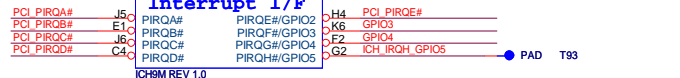
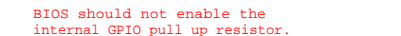
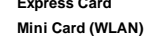
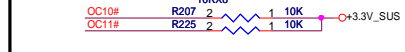
ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



XOR Chain Entrance Strap		
ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff



**Non-iAMT** **ASF 2.0**

+3.3V\_SUS

RP36

1 2 ICH\_SMLINK0  
3 4 ICH\_SMLINK1


\*10KX2\_NC

ICH\_SMBCLK R191 1 2 0 ICH\_SMLINK0  
ICH\_SMBDATA R193 1 2 0 ICH\_SMLINK1

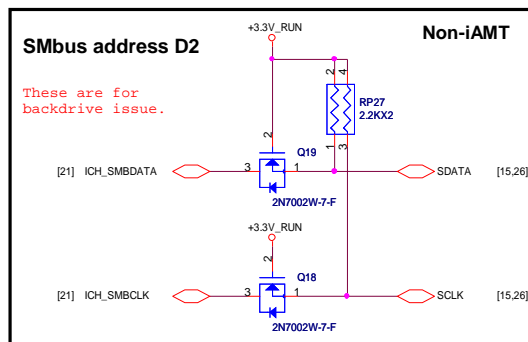
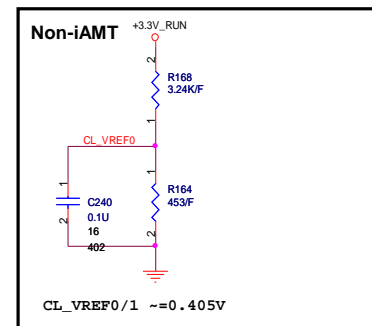
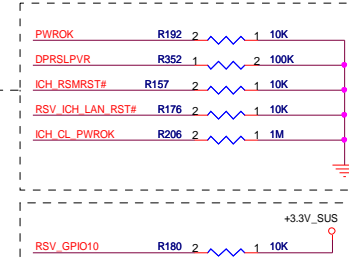
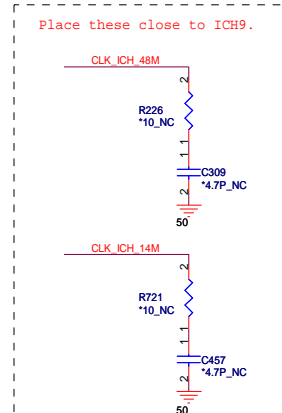
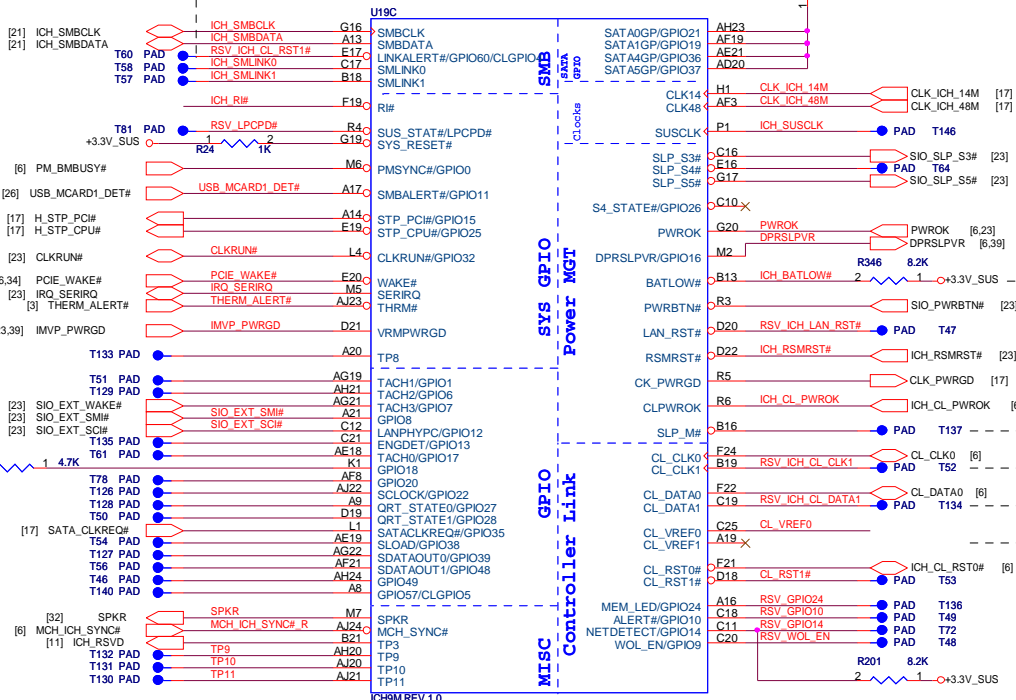
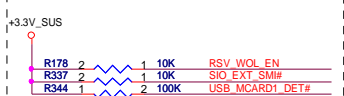
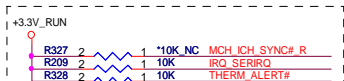
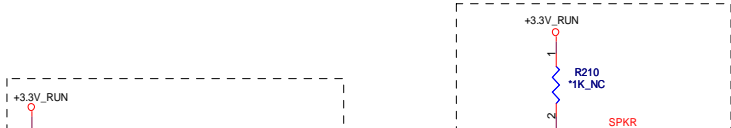
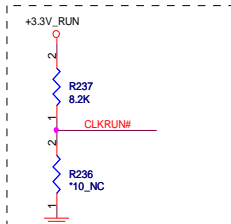
**Non-iAMT**

+3.3V\_SUS

Pin	Signal
R194	RSV_ICH_CL_RST1#
R197	ICH_RI#
R203	SIO_EXT_SC#
R179	PCIE_WAKE#

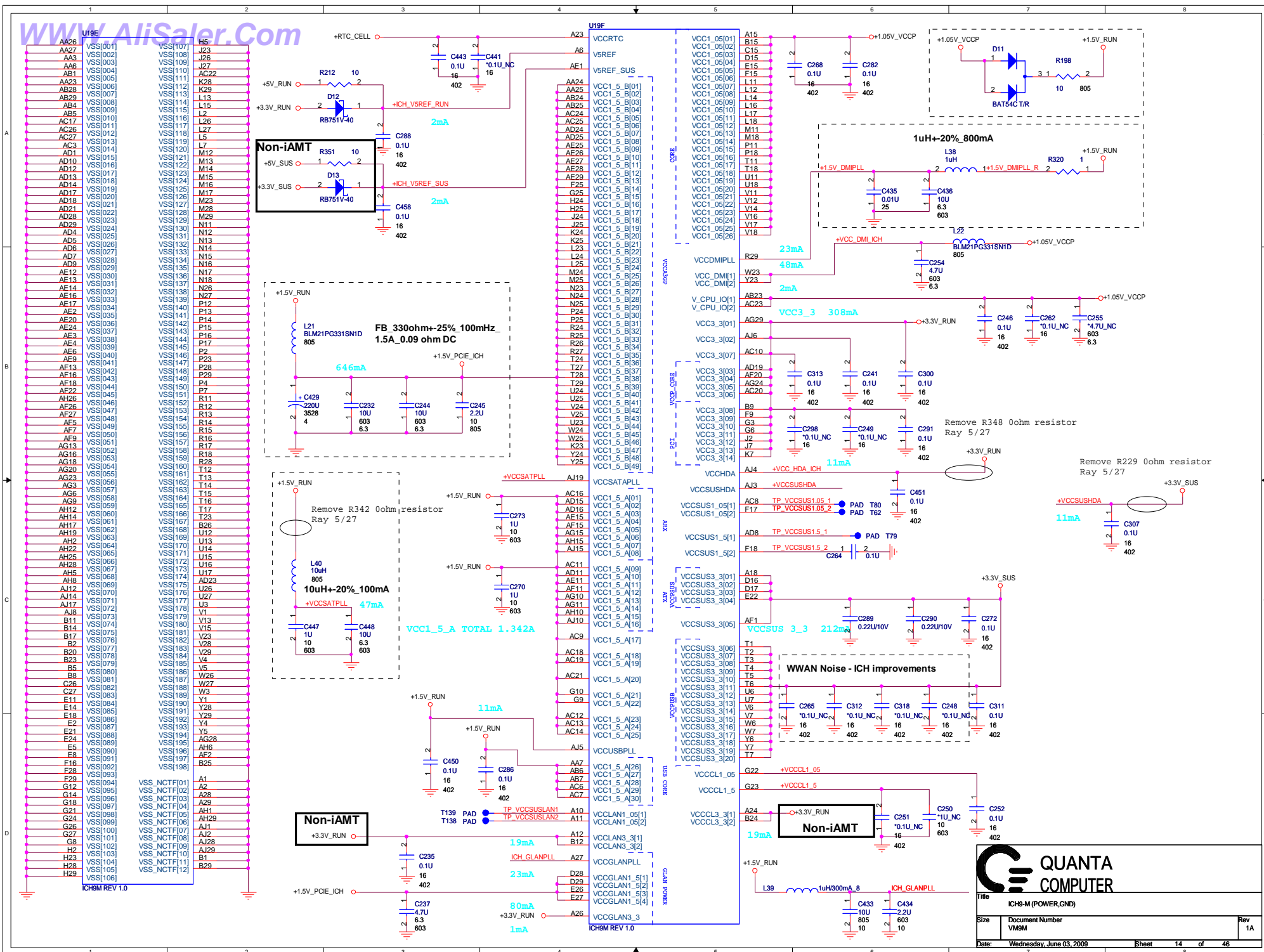


Option to "Disable" clkrun. Pulling it down will keep the clks running.



Non-iAMT

No Reboot strap.	
KR	Low = Default. High = No Reboot.





A is required to route to Top SoDIMM for AMT to function.  
Ch.A SoDIMM needs to be populated for Intel AMT support.

+1.8V\_SUS  
V\_DDR\_MCH\_REF

+1.8V\_SUS

DDR\_A\_DM[0..7]  
DDR\_A\_D0..D3  
DDR\_A\_DQ[0..7]  
DDR\_A\_DQS[0..7]  
DDR\_A\_MA[0..13]

+1.8V\_SUS

+1.8V\_SUS

DDR\_B\_DM[0..7]  
DDR\_B\_D0..D3  
DDR\_B\_DQ[0..7]  
DDR\_B\_DQS[0..7]  
DDR\_B\_MA[0..13]

CN3

VREF

DQ0

DQ1

DQ2

DQ3

DQ4

DQ5

DQ6

DQ7

DQ8

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DQ11

DQ12

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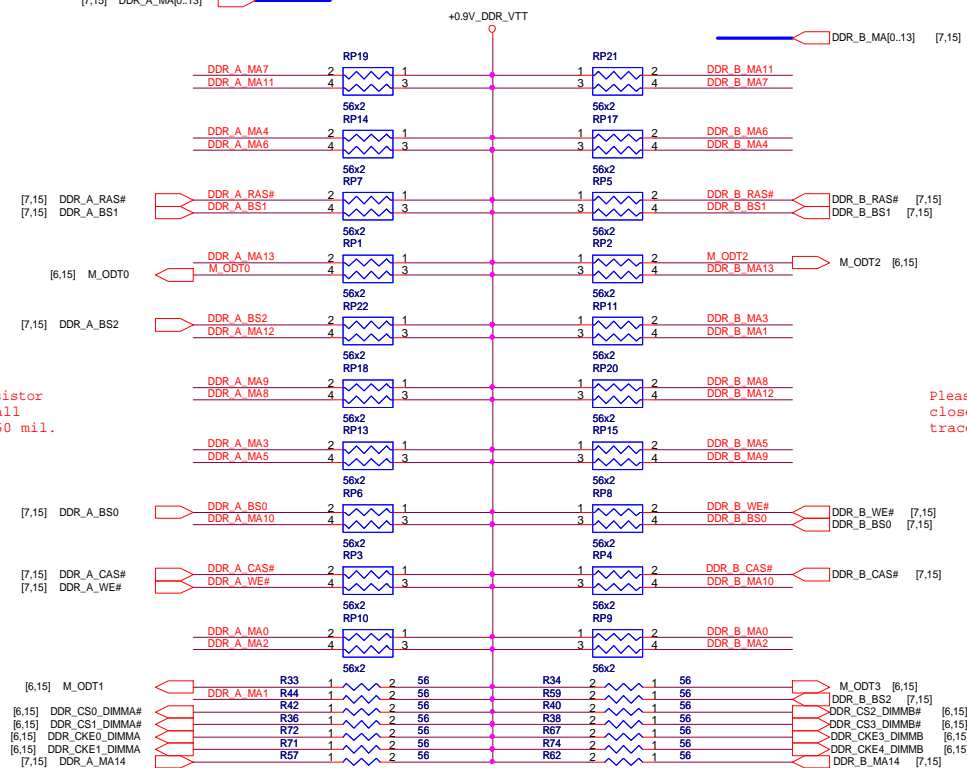
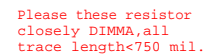
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DQ308

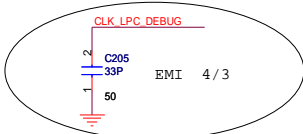
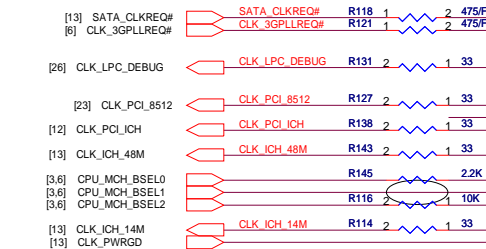
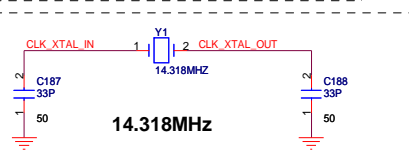
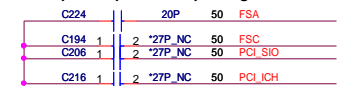
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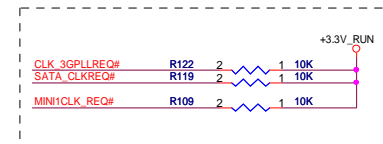
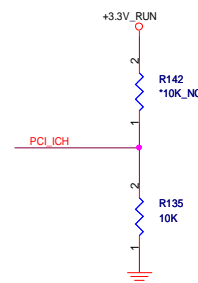
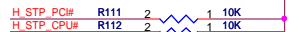
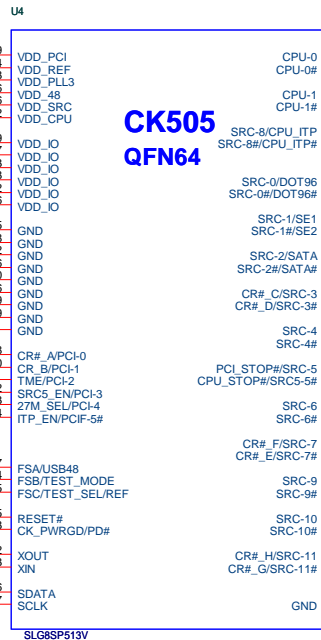
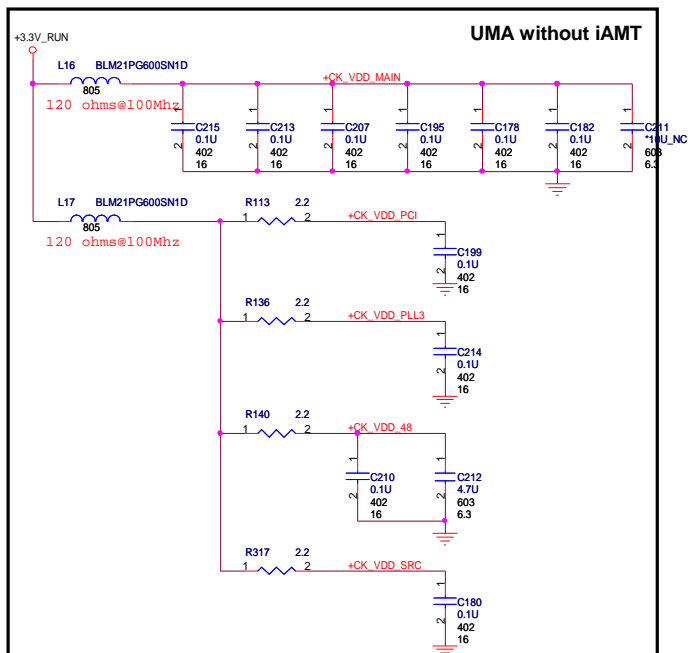
DQ311



Add capacitor pads for improving WWAN.



### UMA without iAMT



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

### 27M\_SEL

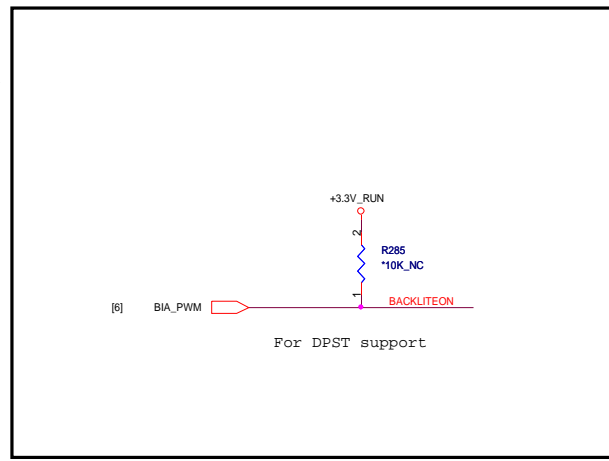
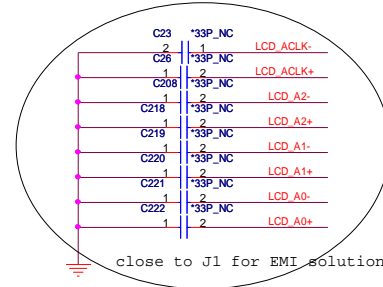
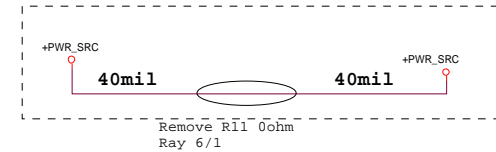
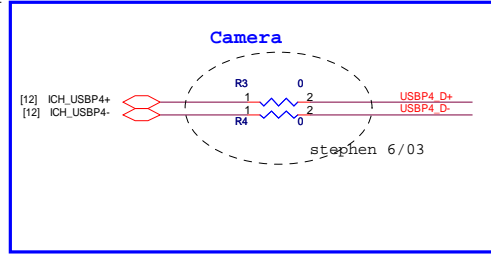
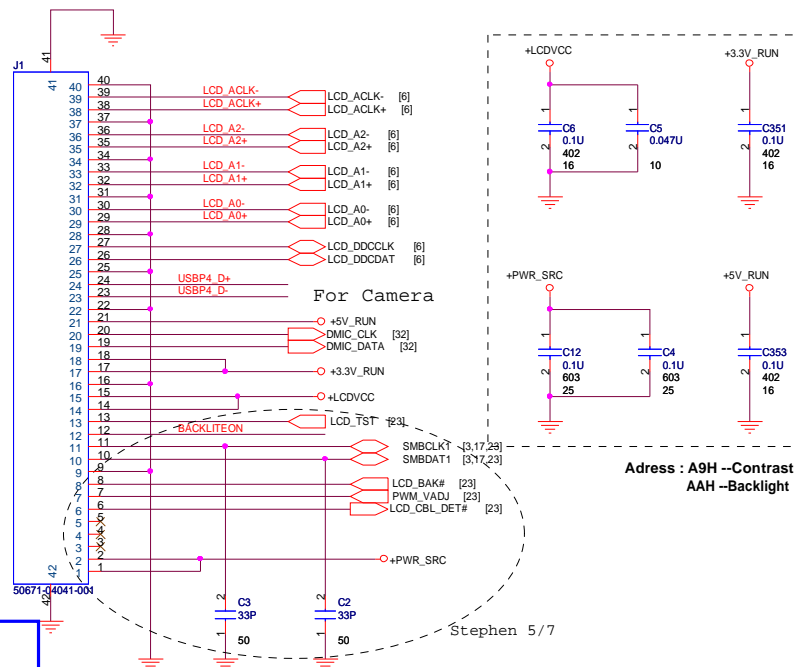
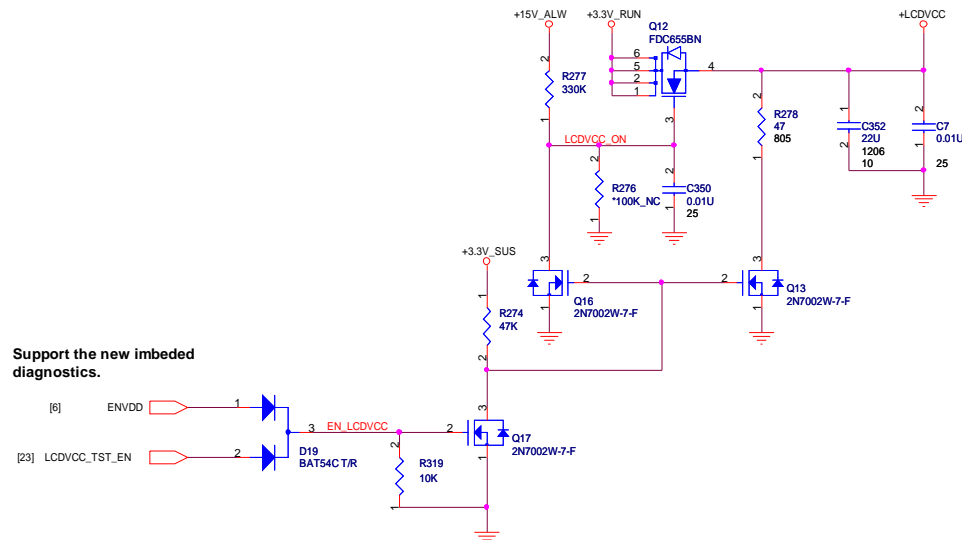
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

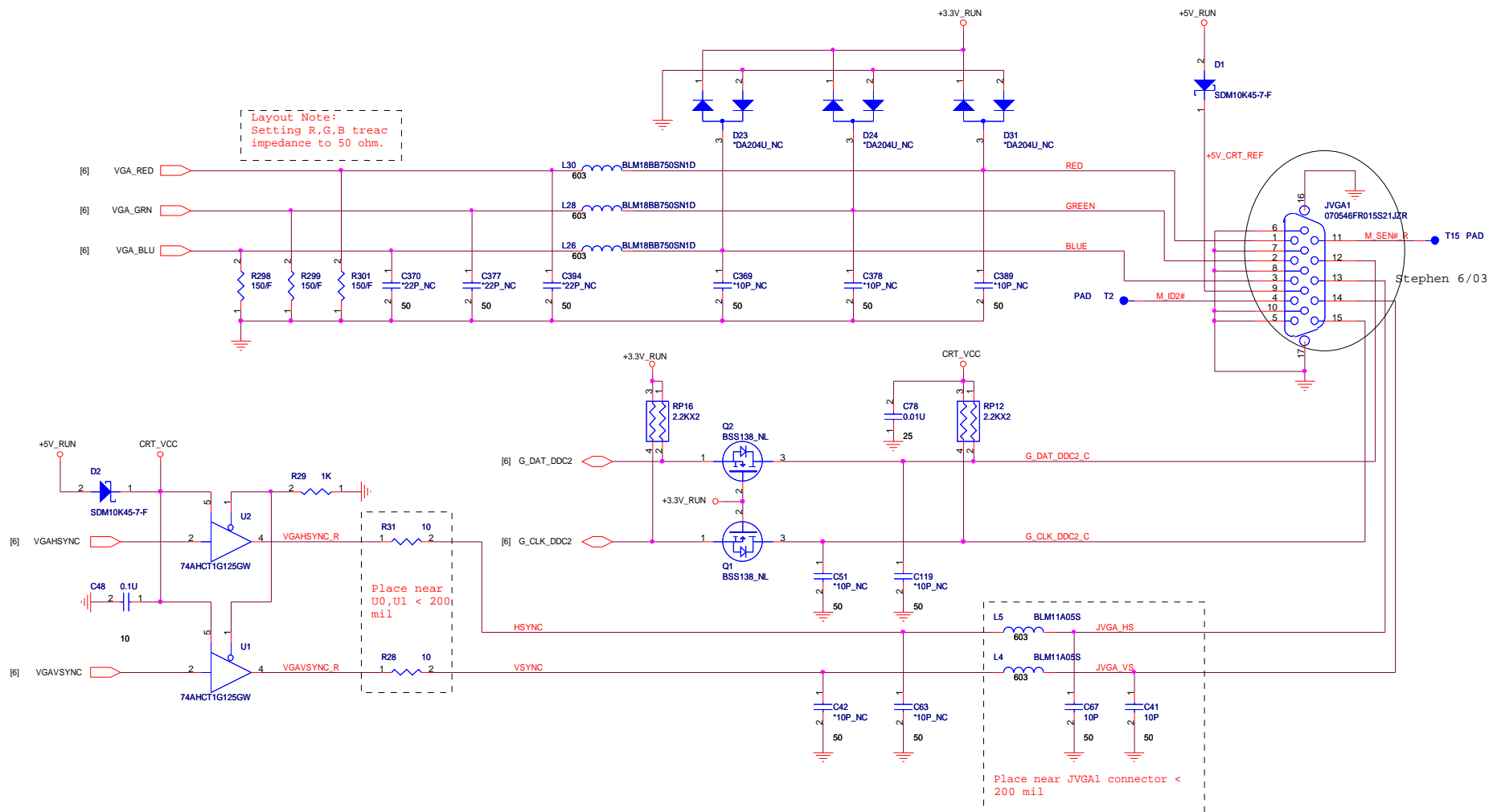



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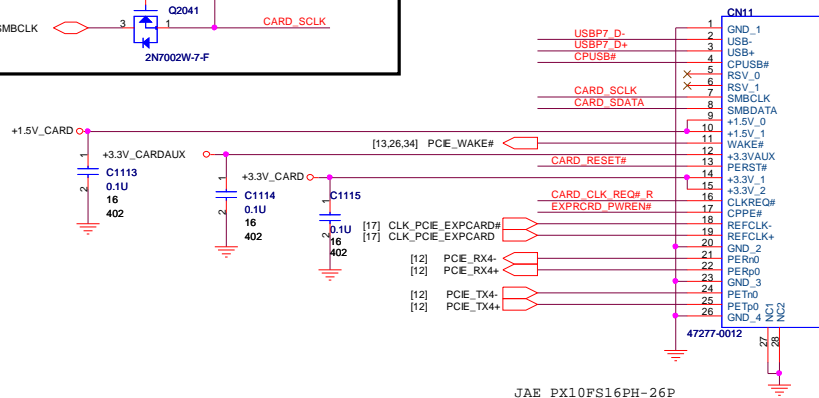
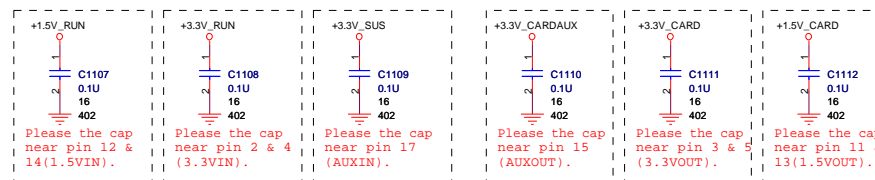
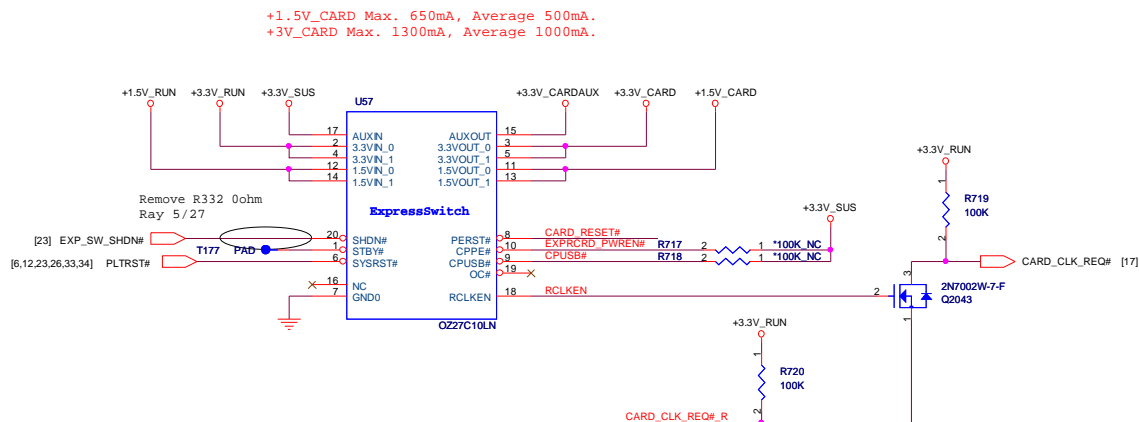
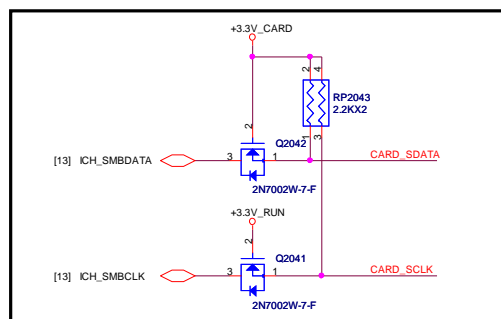
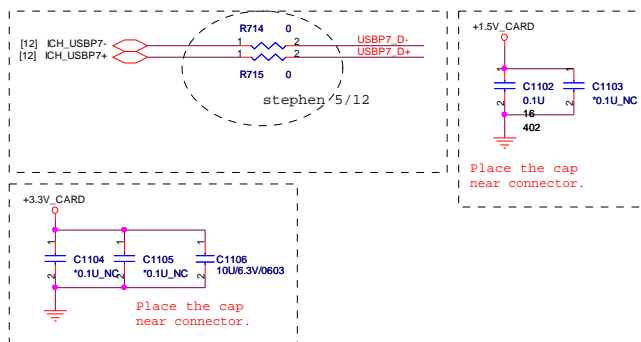




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COMPUTER

Title		
Card Reader-RTS5158E		
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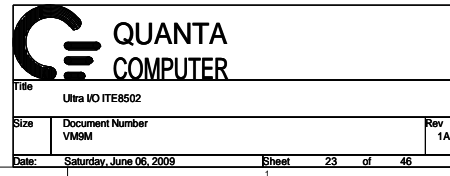
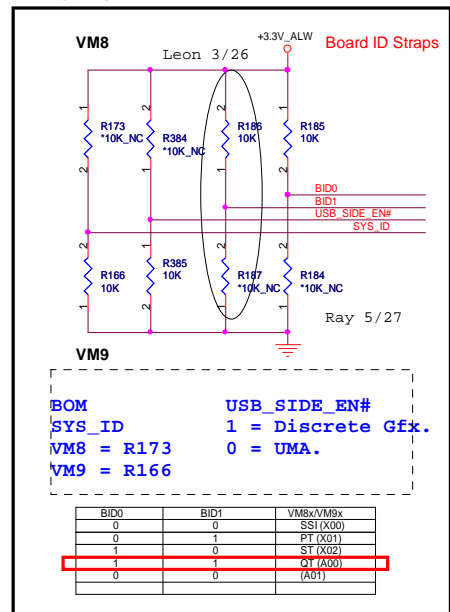
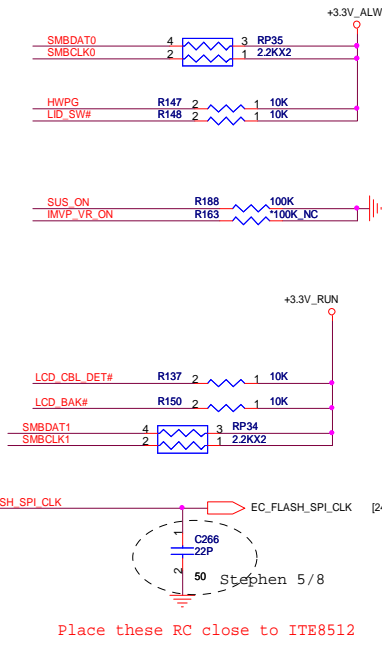
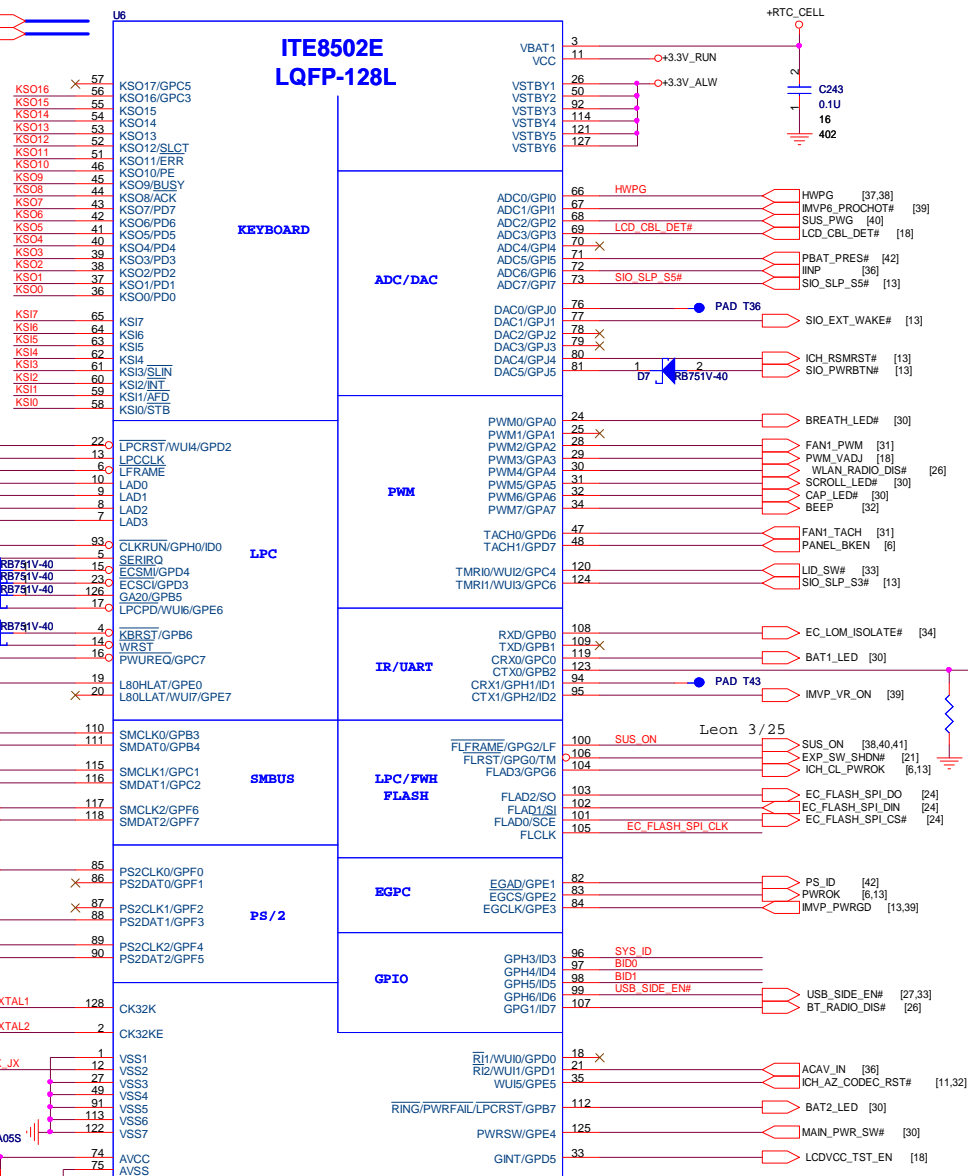
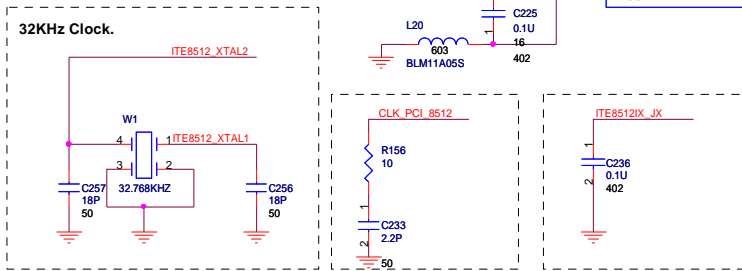
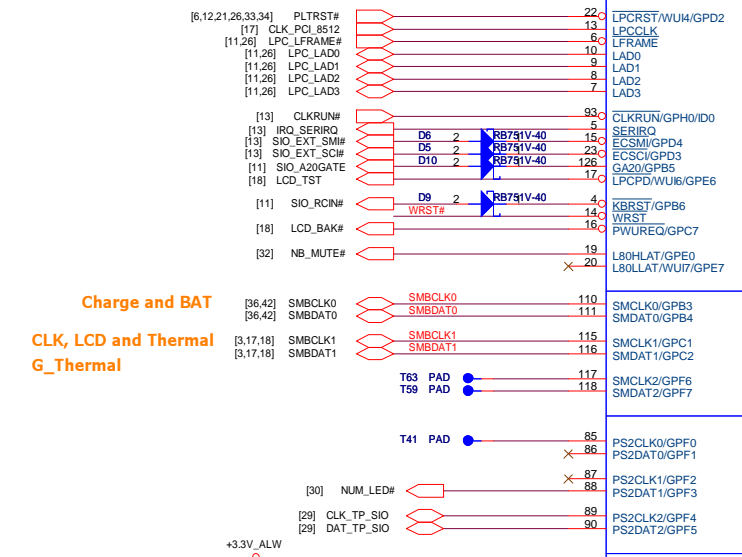
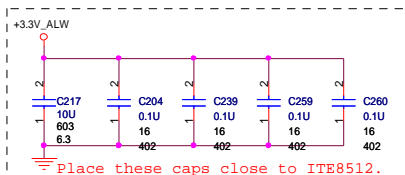


## Express Card

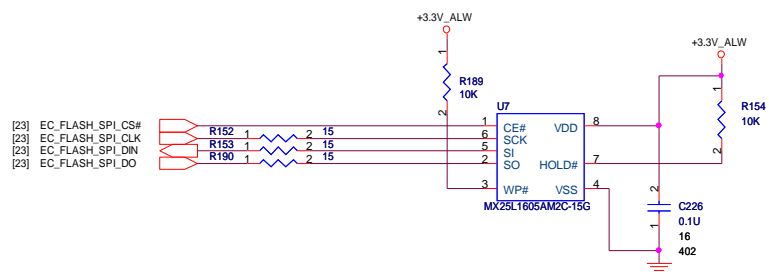


<b>QUANTA COMPUTER</b>		
Title	Express Card	
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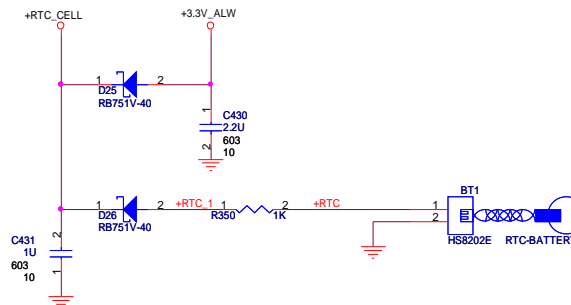
		QUANTA COMPUTER	
Title		black	
Size	Document Number		Rev
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16Mbit (2M Byte), SPI



## RTC BATTERY

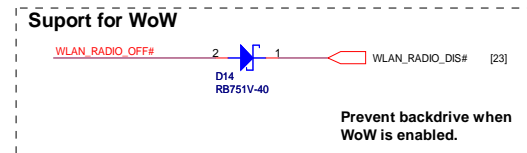
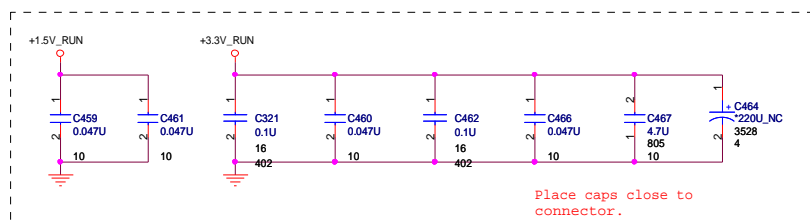
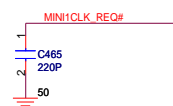
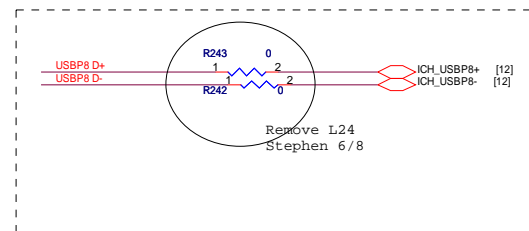
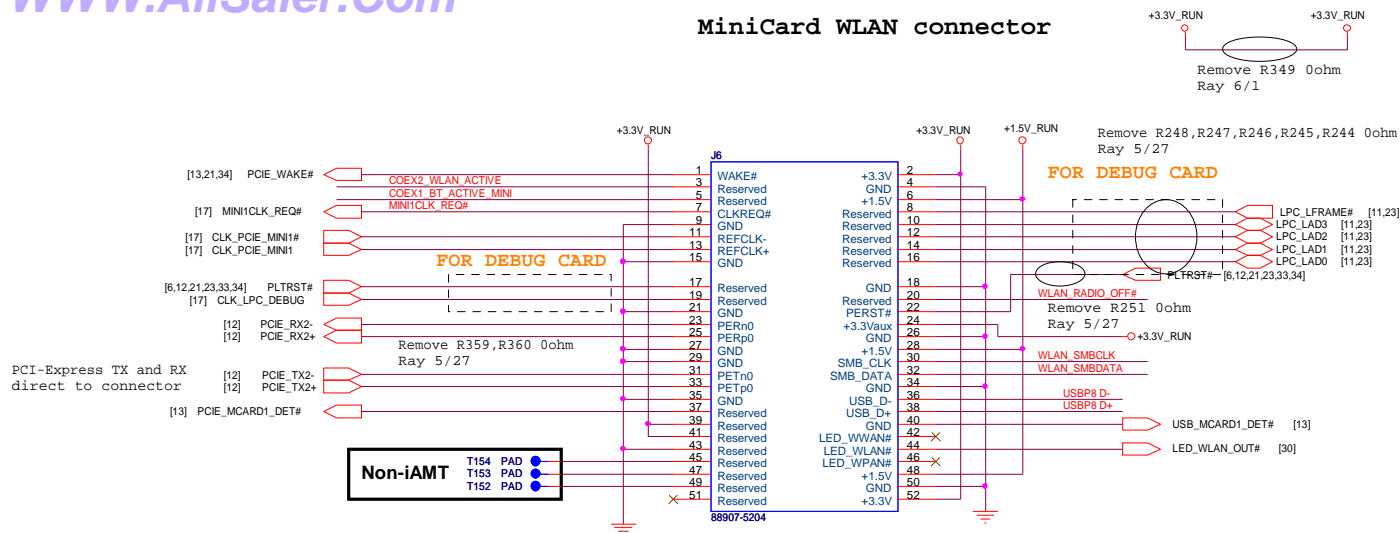




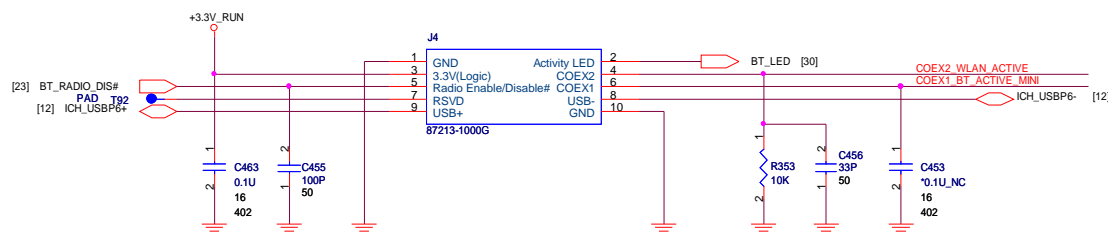
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COMPUTER

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## MiniCard WLAN connector



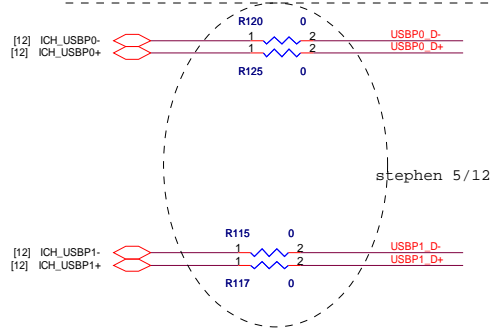
## Bluetooth



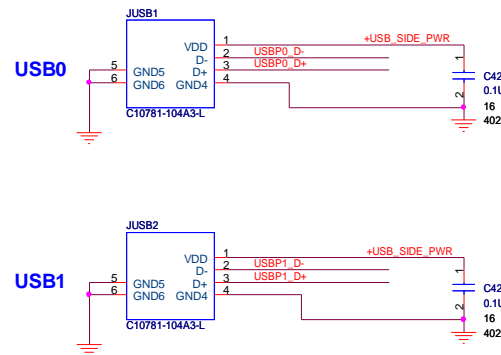
Title			
MDC CONNL			
Size	Document Number		
	VM9M		
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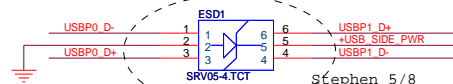
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



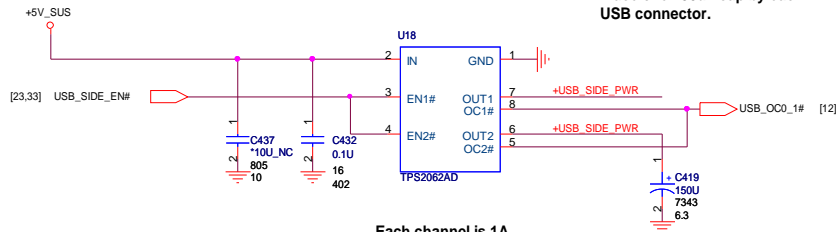
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



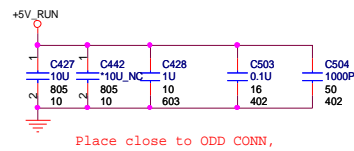
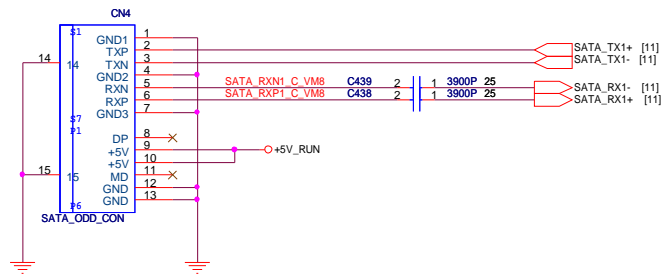
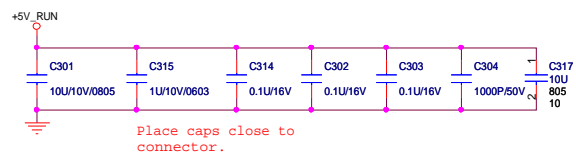
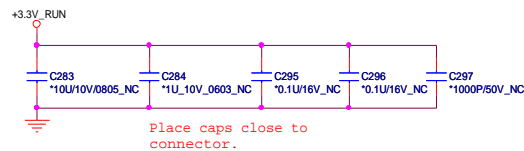
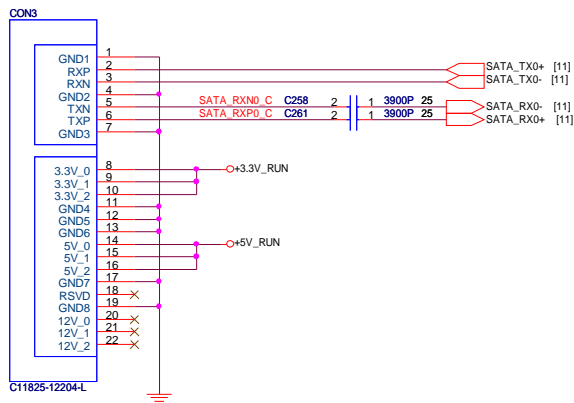
Place ESD diodes as close as USB connector.



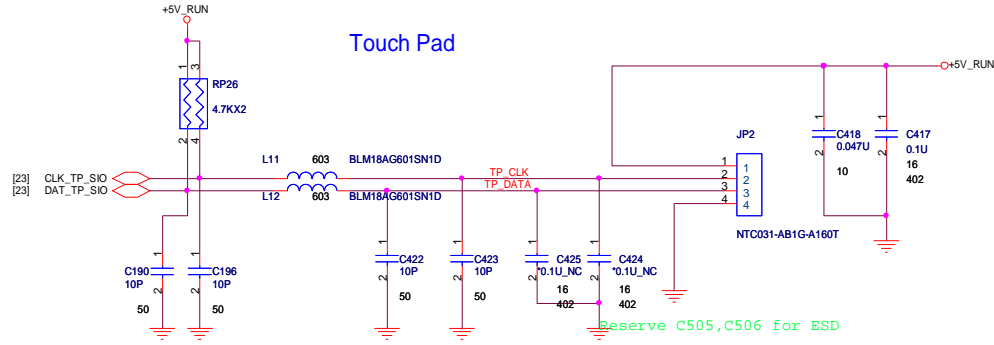
Place one 150uF cap by each USB connector.



# SATA HDD Connector.

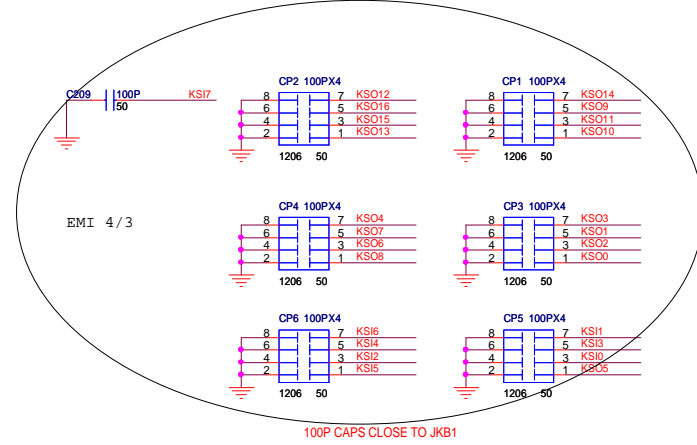
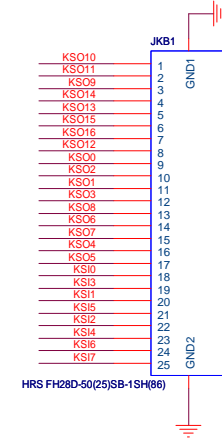


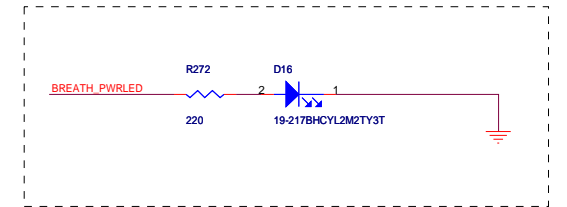
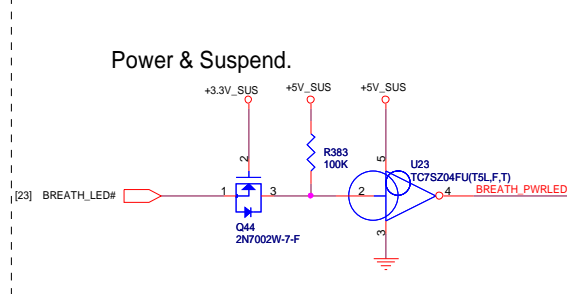
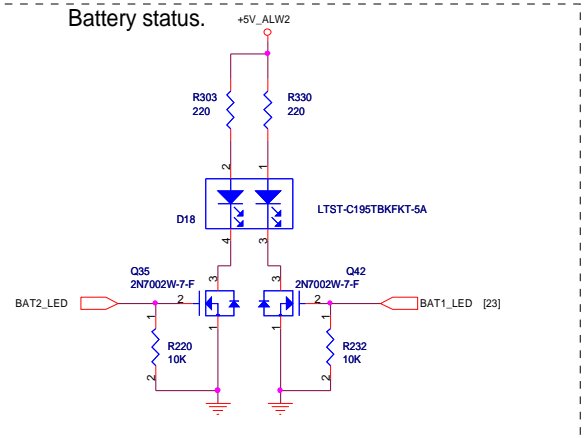
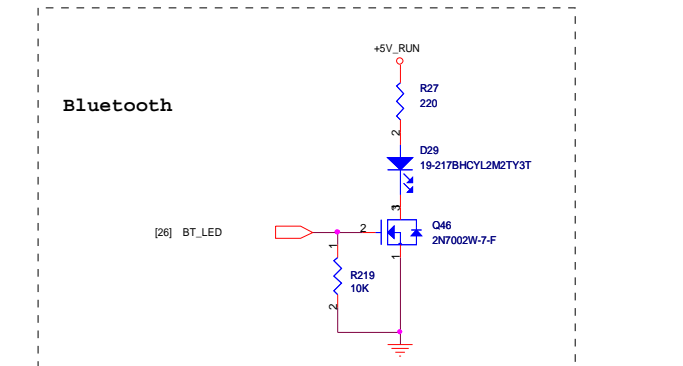
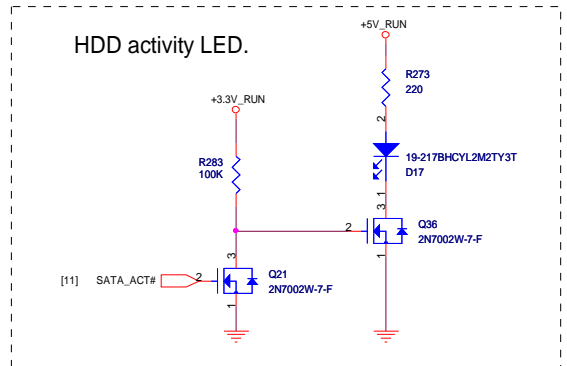
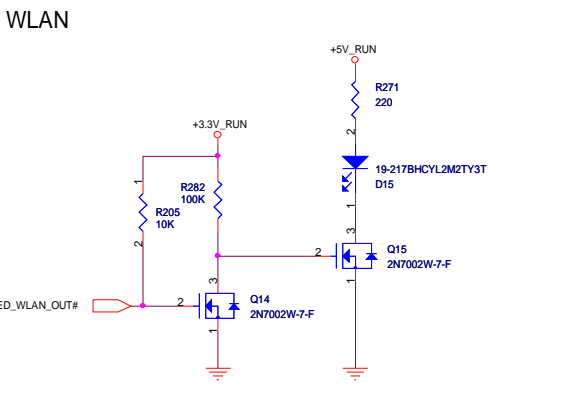
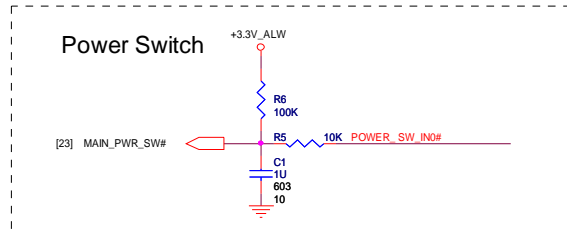
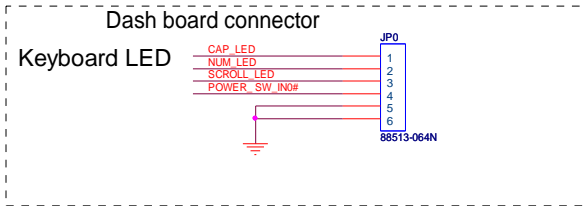
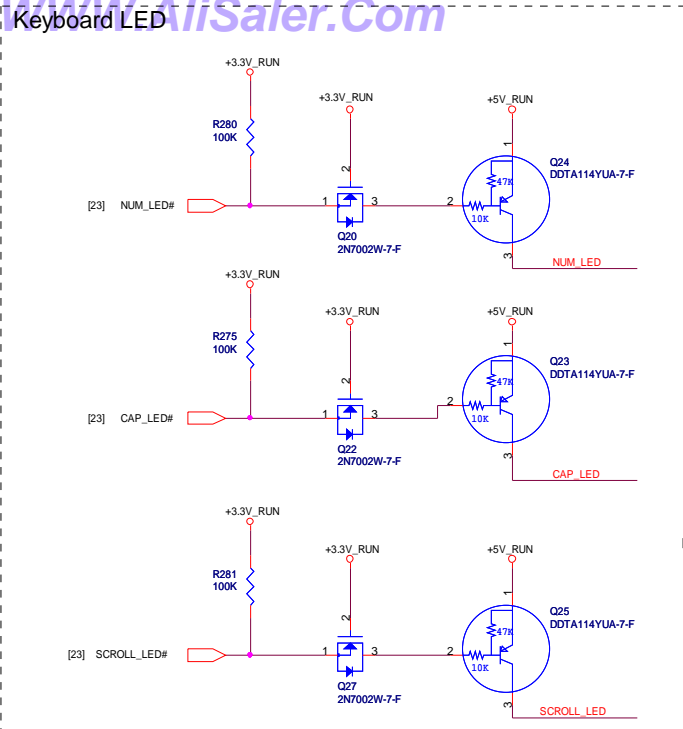
# Touch Pad

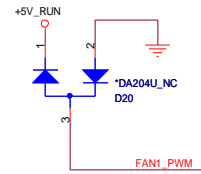


## KEYBOARD CONNECTOR

[23] KSO[0..16]  
[23] KSI[0..7]

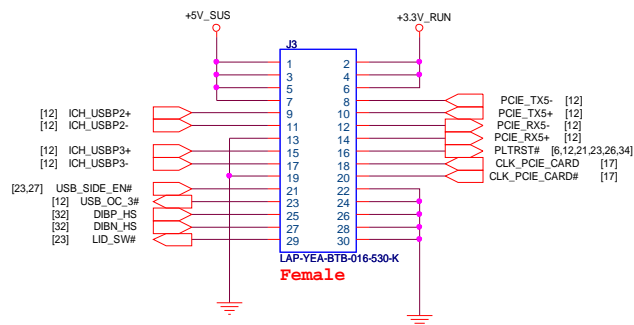
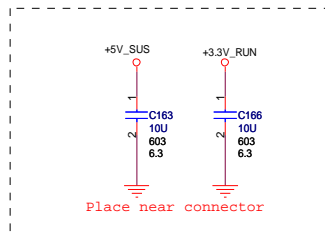












Board to board connector (Modem Card + Cardreader+1394a+ 2 USB Port)

A

B

C

D

E

4

4

3

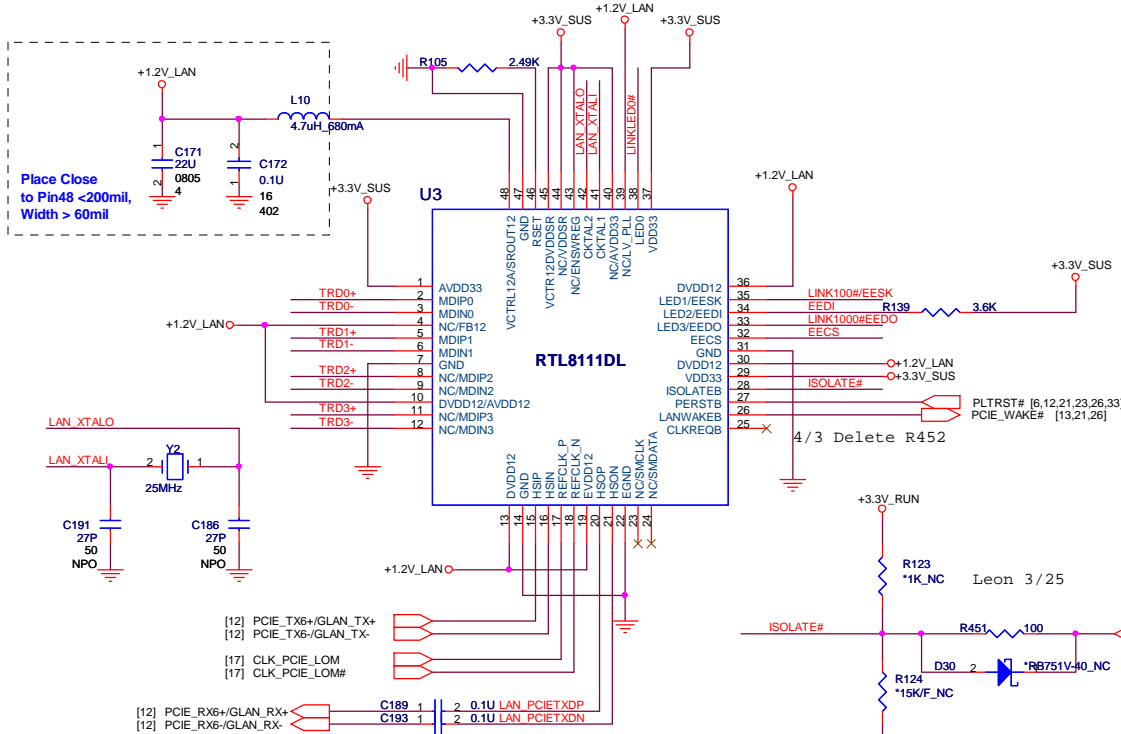
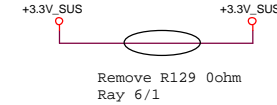
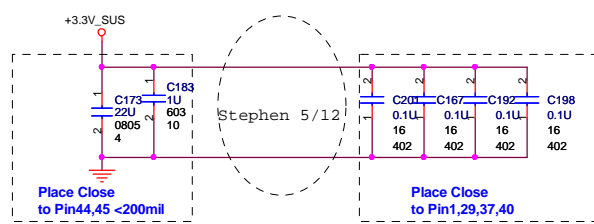
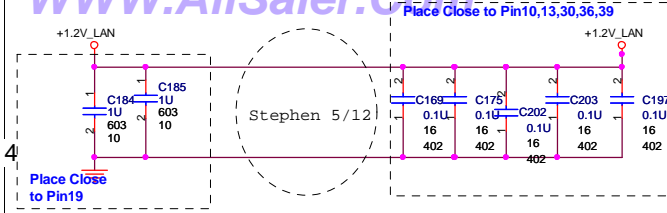
3

2

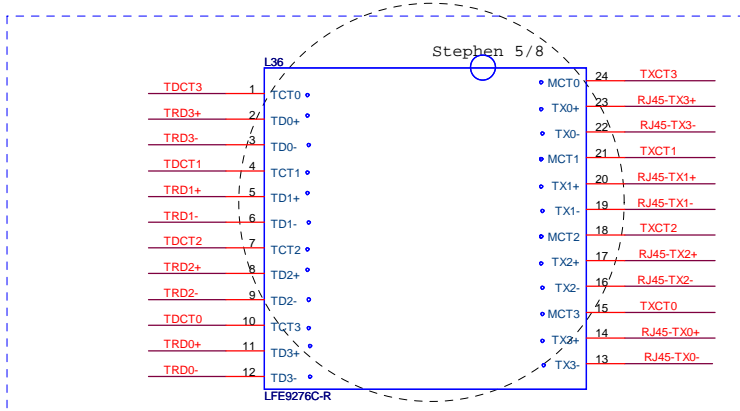
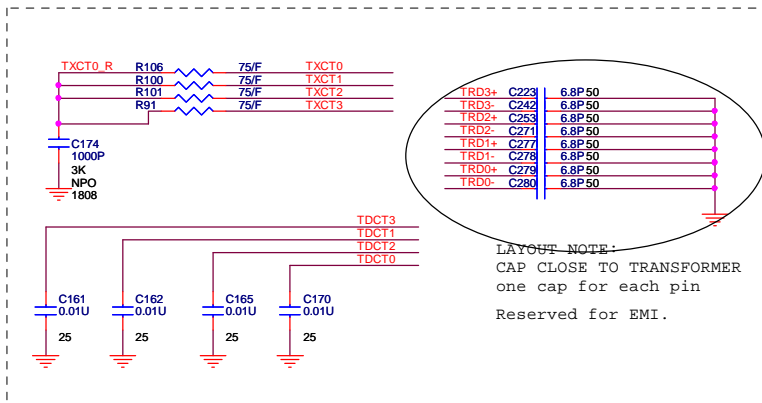
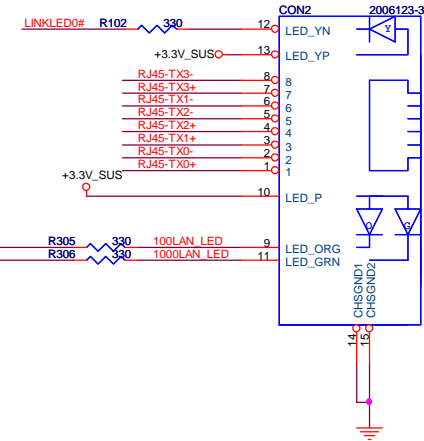
2


1

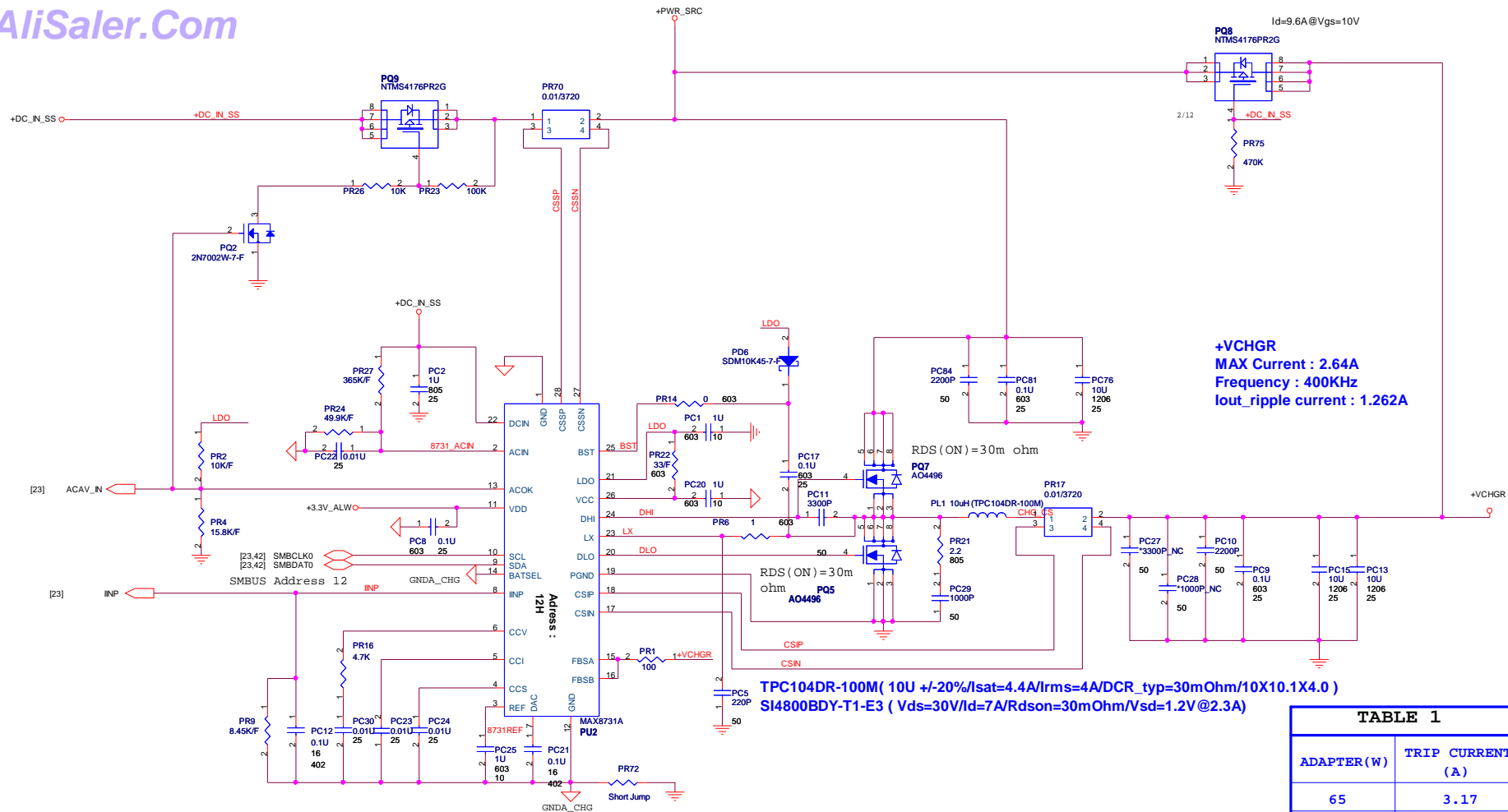
1

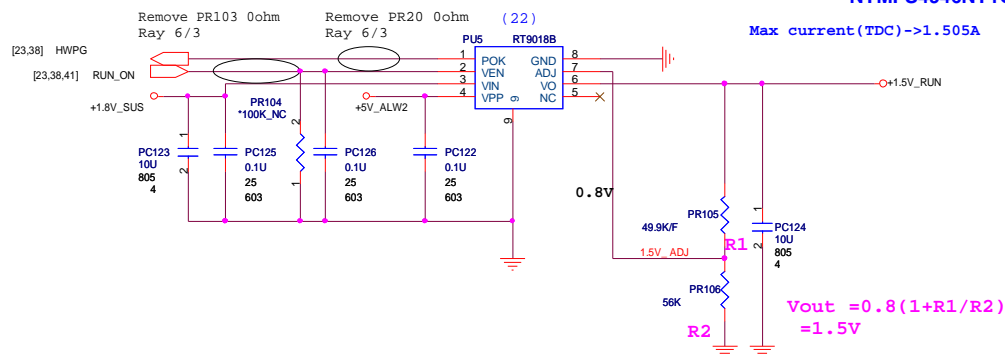
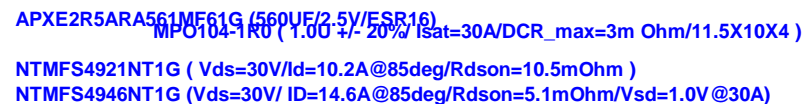


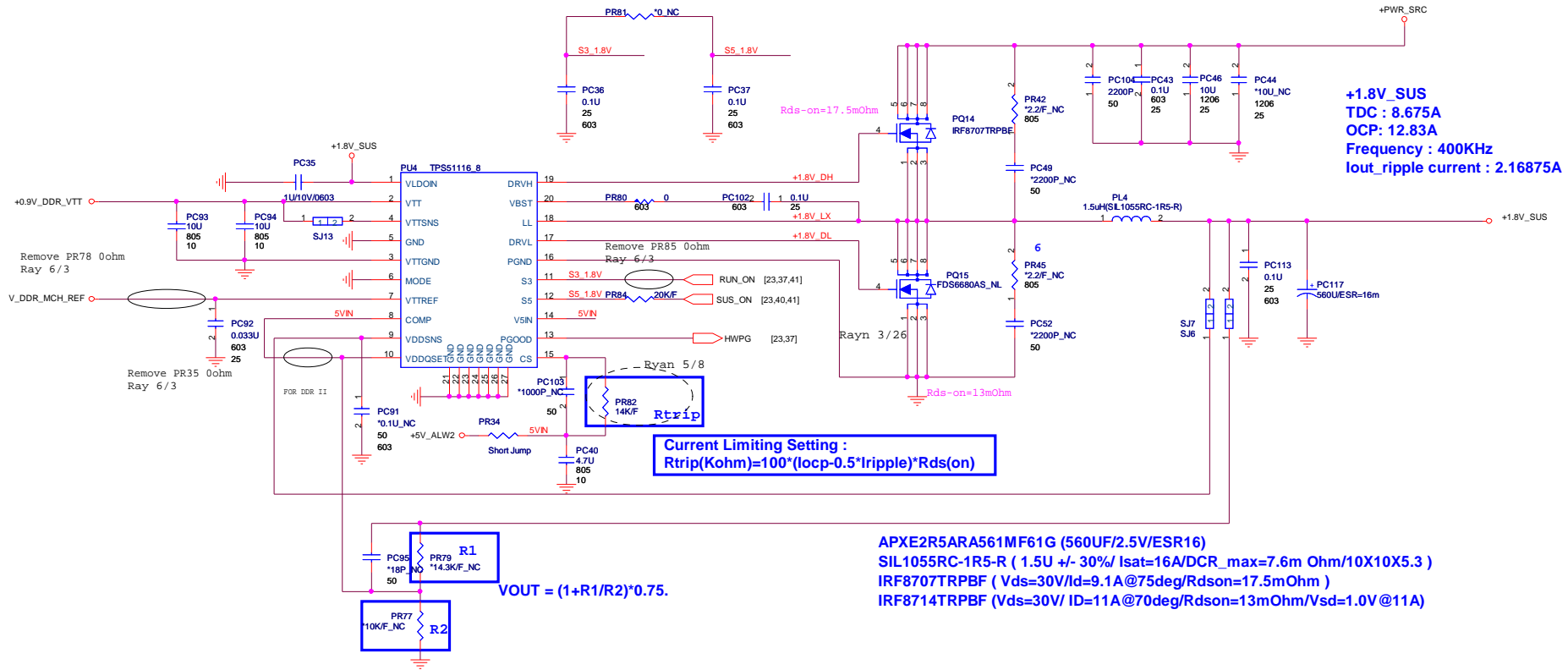
RJ-45 Connector



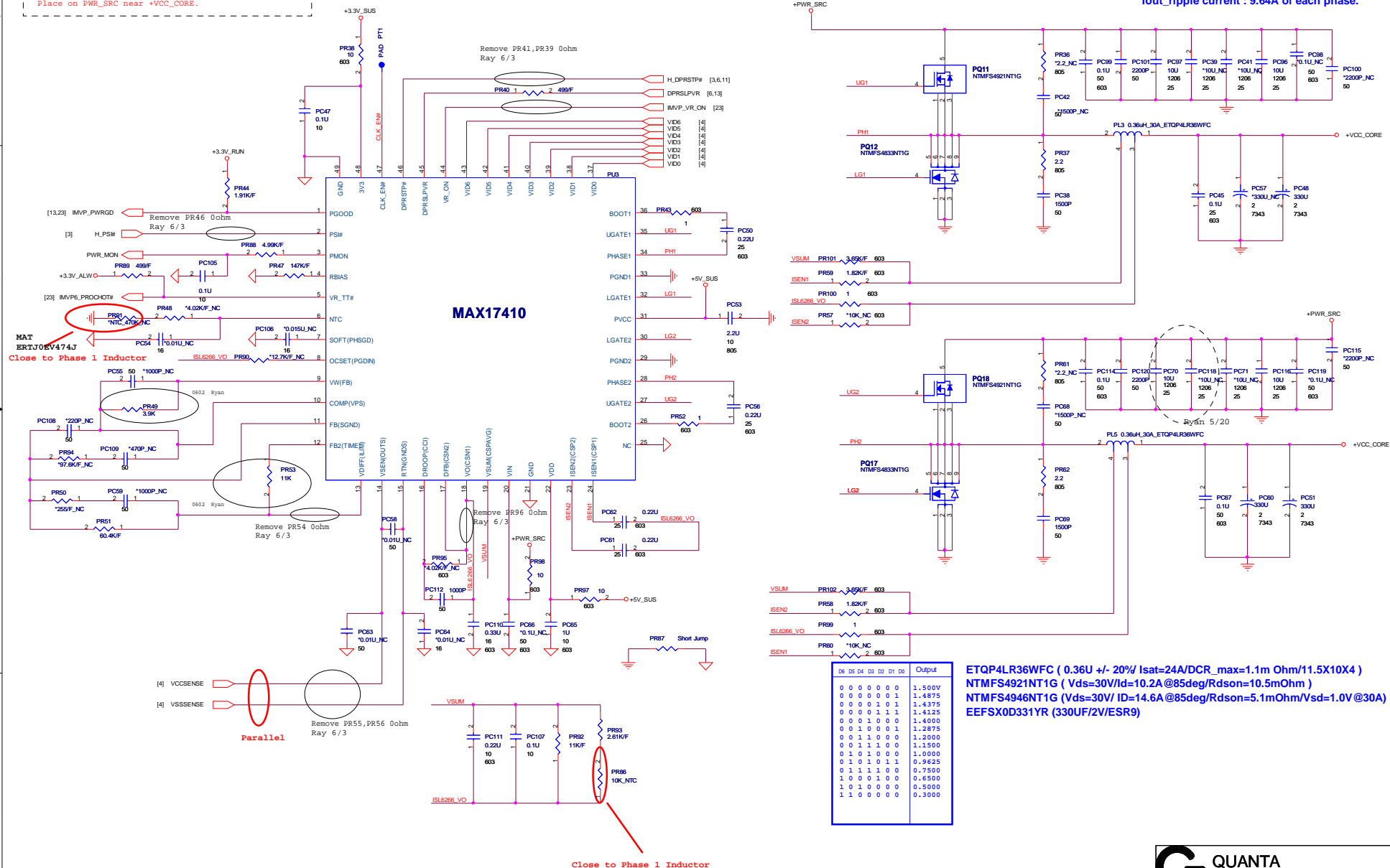
 QUANTA COMPUTER		
Title System Reset Circuit		
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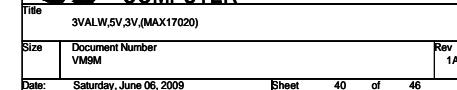
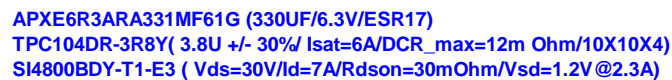


Layout Note:  
Need to add 100uF cap on PWR\_SRC for cap singing.  
Place on PWR\_SRC near +VCC\_CORE.

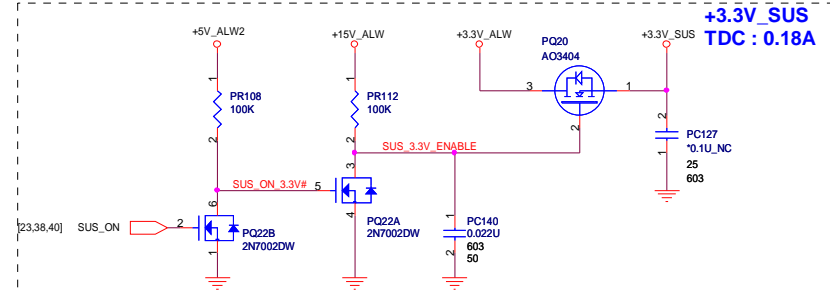
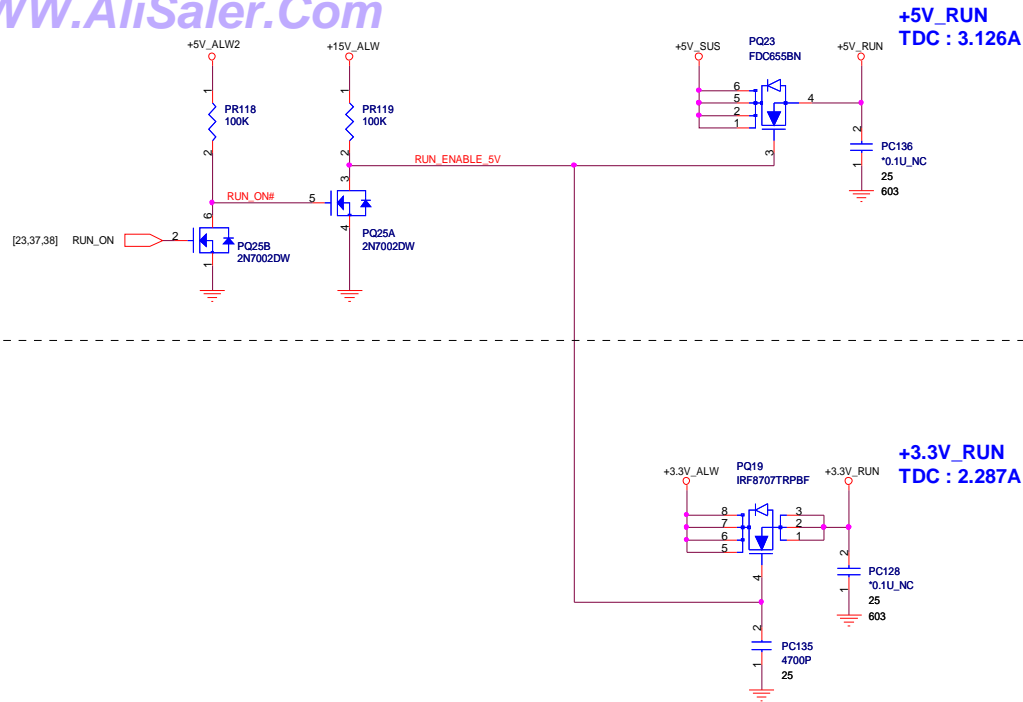


QUANTA  
COMPUTER

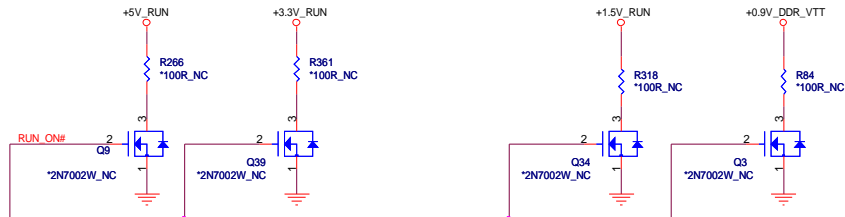
Title		CPU_Core_2Phase (MAX17410)	
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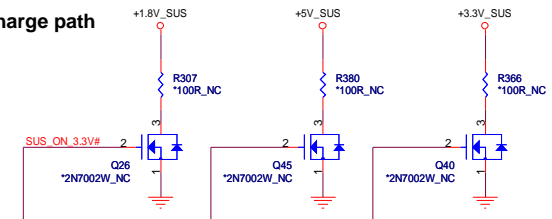




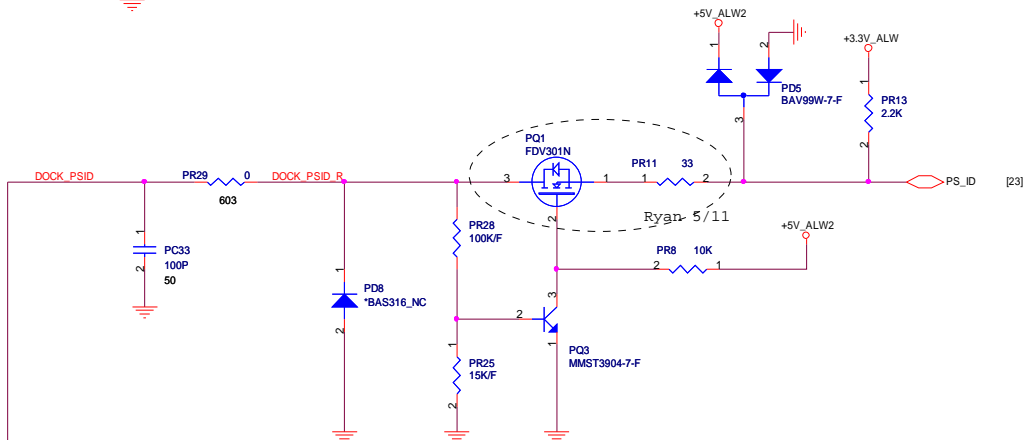
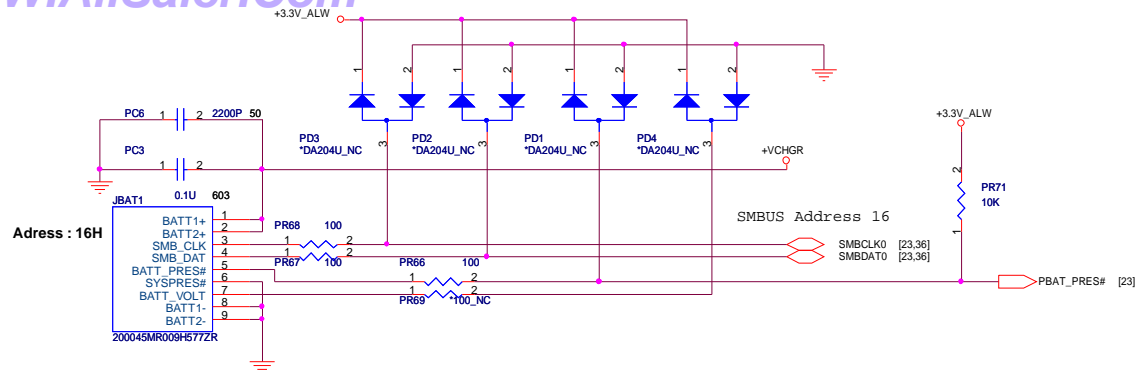
#### Reserve discharge path



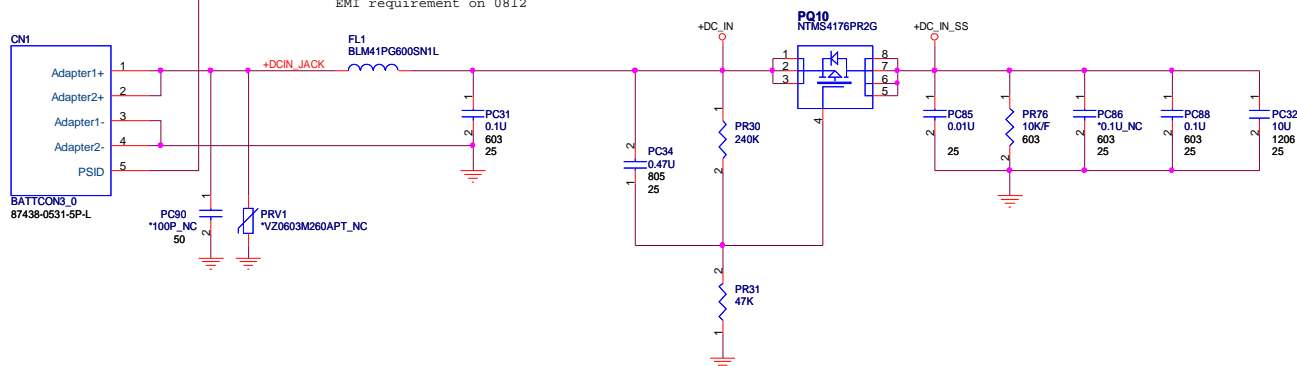
#### Reserve discharge path

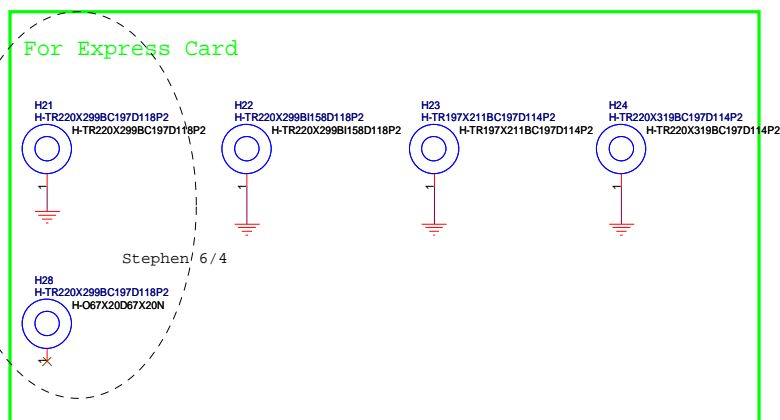
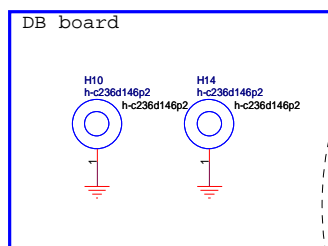
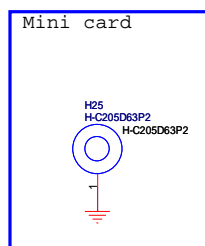
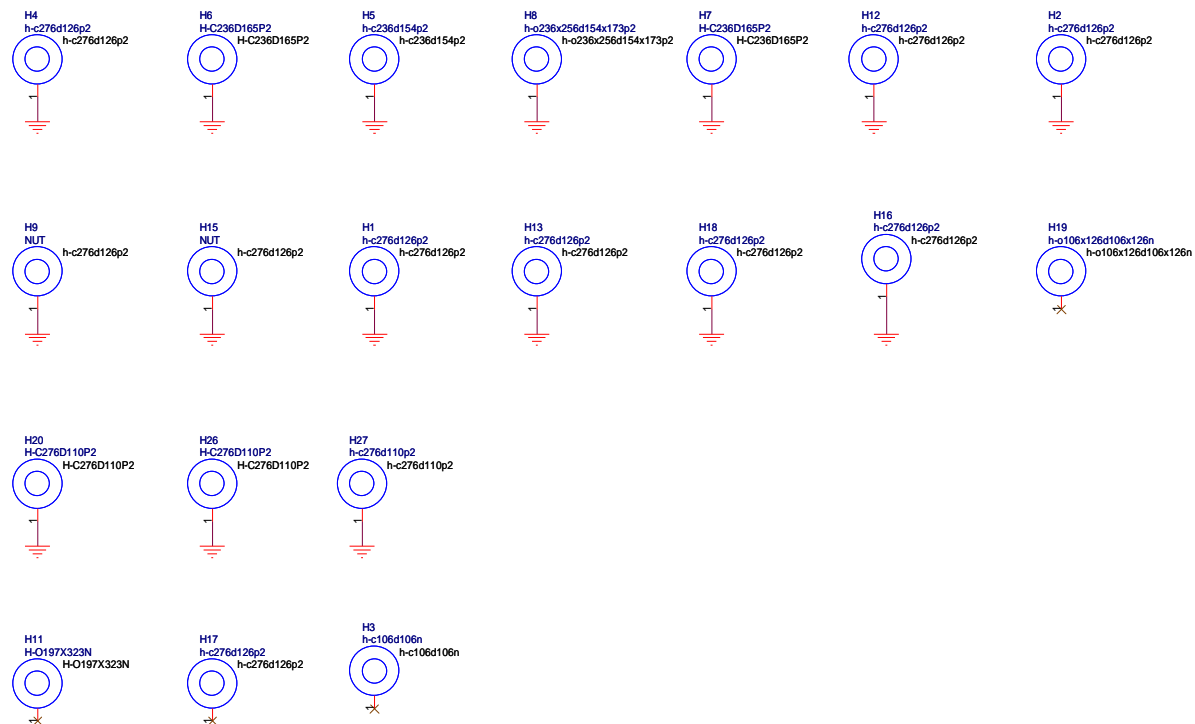



Title		
RUN POWER SW		
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Change Value per GG updated  
EMI requirement on 0812





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